



## Polysilicon CMP

By Robert L. Rhoades, Ph.D. and Terry L. Pfau  
CMP-MIC March 2007 – Fremont, CA





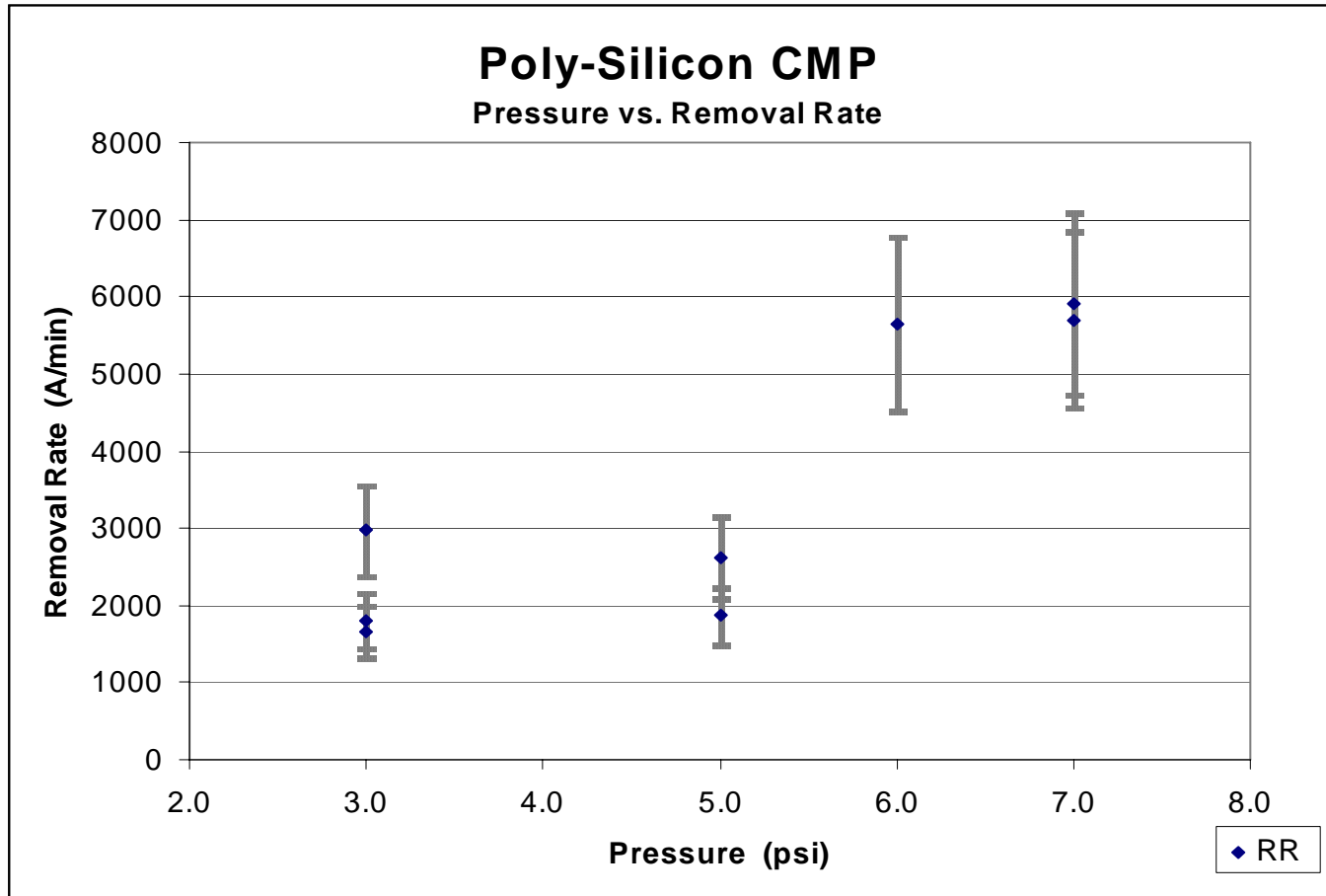
- **Polycrystalline Silicon**  
(polysilicon, p-Si, poly-si, poly, etc...)
- **History and Early Application**
- **Examples of New Applications for Polysilicon**
- **Future Evolution**



- Polycrystalline Silicon (polysilicon)
  - An early application for poly was the replacement of aluminum as the material for the control gate of a MOS transistor. Poly gate electrodes were 3 or 4 times faster, had lower leakage currents, could tolerate higher temperatures, and were more reliable than aluminum gate electrodes.
  
- Emerging Applications
  - Damascene Style Polysilicon
    - Similar to Cu damascene processing
  - Structural Components in MEMS Devices
    - Large feature devices (several hundred microns)
    - Large step heights (tens of microns)
  - Surface Preparation
    - Reduce surface roughness (Ra) for direct wafer bonding, optical surfaces, or other specialized purposes



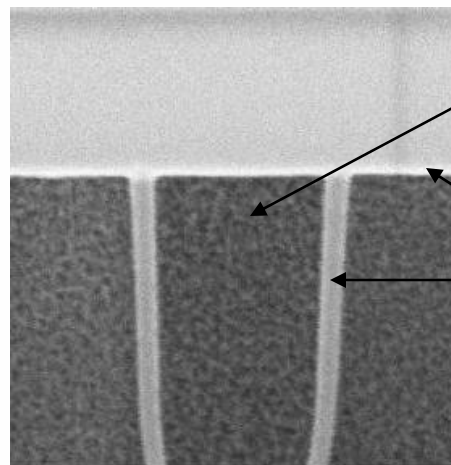
- Polysilicon CMP has a wide range of requirements for its applications. The consumable sets and processes chosen for the applications are just as wide ranging.
  - **Most of the processes shown in this paper utilize an industry standard planarizing pad with a newly developed slurry specifically formulated to polish polysilicon without differential grain boundary highlighting.**
- The following graph of removal rate and polish pressure has been generated to show the removal rates that have been used for the different applications. The graph “error bars” have been used to show the range of removal rates achieved for the most common polish pressures used.
- The removal rate range depends on the tool type, pad, slurry, pressure, and rotational speeds that have been chosen for the specific application.



# “Damascene Style” Polysilicon

Example Parameter	Value or Description
Top layer material	Polysilicon
Bottom layer material	Oxide (undoped)
PolySi removal rate	4100 Ang/min
Selectivity (PolySi:Oxide)	>100 : 1
Planarization Efficiency	> 99%

- The damascene style involves etching a pattern into an oxide film then growing a layer of polysilicon to fill the inlaid features. The polysilicon thickness depends on the specific application, but is frequently 1 to 2 microns thick.
- These can be relatively long polishes but still need to minimize the feature dishing. In general a two step process will be used to remove and clear the top layer of polysilicon.
- Most often the bulk of the poly removal will use a higher polish pressure with removal rate of 5000 to 6000 Å/min to remove most of the overburden then reduce to a lower polish pressure of 1500 to 3000 Å/min to clear the last of the poly film.



Polysilicon plug

Thin oxide layer  
(capping oxide added for SEM prep)



Example Parameter	Value or Description
Top layer material	Polysilicon
Bottom layer material	Pattern or Si Substrate
Polish Pressure	6 – 8 psi
PolySi removal rate	5.5k – 6.5k Å/min
Planarization Efficiency	>90%
Surface Roughness	<50 Å

- MEMS technology is an example of planarizing large polysilicon structural features. The polysilicon features can be hundreds by hundreds of microns and up to tens of microns in step height.
- These can be very long polishes requiring the removal of several microns of polysilicon to reduce step heights and planarize the surface.
- CMP goal is to reduce the step heights and leave the polysilicon surface planarized, often with minimum surface roughness as a secondary requirement.



Example Parameter	Value or Description
Top layer material	Polysilicon
Bottom layer material	Pattern or Si Substrate
Polish Pressure	3.0 psi
PolySi removal rate	1.0k – 2.0k Å/min
Surface Roughness	<10 Å

- Direct wafer bonding (DWB) and optical surfaces are two examples that require clean smooth surfaces.
- This type of polish is generally short and usually only requires a minimum removal of 1000 to 1500 Å of polysilicon to achieve a sufficiently low Ra. Removal rates are kept low and grain boundary highlighting must be controlled.
- CMP goal is to reduce surface roughness and leave the polysilicon surface with a clean “mirror like” surface in preparation for additional processing. Typical incoming Ra’s are 50 to 150 Å and typical post polish Ra’s are < 10 Å.



**CMP FastForward™**

## Future Evolution

- The use of polysilicon CMP continues to increase in advanced device designs of all types. This trend is expected to continue.
- Many of these applications require smooth planarized surfaces. A wide range of repeatable CMP processes have been developed to address these applications with an approach that is flexible enough to enable further adaptation with relative ease.

### References

- R. Rhoades, "Evolution of CMP for New Materials and Applications." ECS Symposium (invited talk), October 2006.
- P. Van Zant, "Microchip Fabrication : a practical guide to semiconductor processing." McGraw-Hill, 1997.

## Thank you

### Contact Info:

**Robert L. Rhoades**

Tel: 602 426-8668

Fax: 602 426-8678

rrhoades@entrepix.com

### Contact Info:

**Terry L. Pfau**

Tel: 602 571-2962

Fax: 602 426-8678

tpfau@entrepix.com

