CMP chemistry and materials challenges for ultra low-k integration

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ABSTRACT

Advanced semiconductor devices have evolved over recent years through a series of steps that included the introduction of both copper metal and low-k dielectric materials for the interconnect module. As designs continue to push toward faster speeds and smaller linewidths (65, 45, 32 and 22nm), the dielectric constant (k) required at each successive technology node is projected to continue dropping toward effective k-values of 2.5 or below. The new materials required to reach these values are generally referred to as ultra low-k, or ULK, dielectrics. Developing such ULK materials is an incredible challenge, but several candidate materials are now available. However, integrating them successfully into a reliable CMOS device manufacturing flow is proving to be extremely difficult, especially with regard to the CMP process module.

This article reviews recent progress and issues related to integrating ULK dielectrics, particularly as related to chemistry and interactions with CMP and post-CMP cleaning. In this context, the ULK material must first be mechanically and chemically stable during all phases of the CMP process. For some integration schemes, this may include direct exposure of the ULK surface to the final step of slurry, which is used to polish away the thin barrier metal and expose the dielectric below. The post-CMP cleaning chemistry will also be in direct contact with the ULK film and must not only perform the necessary function of cleaning away particles and other residuals from the polishing process but also must not itself damage or inadvertently alter the ULK material. In order to be successful at achieving future design targets, the combined system of materials, chemistries and processes must be integrated in a way that allows adequate repeatability and control for manufacturing. This will continue to demand close cooperation between designers, integration teams, process engineers, ULK developers, CMP consumables suppliers, and post-CMP cleaning chemistry suppliers.

Background

Arguably the most referenced trend in the semiconductor industry is 'Moore's Law,' which is interpreted as saying that the number of transistors in an integrated circuit will double every 18-24 months (at roughly the same cost). This trend has held for over 30 years in spite of industry upturns and downturns, global economic conditions, technical hurdles, and all other factors that might have derailed it (see Figure 1) [1]. An impressive series of technology advancements have helped maintain momentum year after year, including the development of entirely new process technologies such as chemical mechanical planarization (CMP).

Materials and integration

In 1995, Mark Bohr of Intel presented his classic paper [2] in which he predicted that both the metal wiring
(Al) and the insulating dielectric material (SiO₂) would have to change within a few years to meet the ITRS Roadmap requirements and maintain the gains prescribed by Moore’s Law. Subsequently, Sematech published a supplier list in 1996 in which 155 potential low-k candidate materials were identified for integration into the next generation interconnect module. While many of these original candidates have since been proven to be impractical, there are numerous dielectric films now available under various trade names in several categories of materials (see Table 1) along with their typical range of k-values.

In 1997, IBM first announced successful integration of Cu for metal wiring at the 220nm node, replacing Al, and in 2000, IBM further announced SiLK as the intended low-k dielectric for the 130nm node [4]. In the nine years since that announcement, numerous companies have begun using Cu interconnect with various attempts at low-k dielectrics. Most of these efforts failed to reach high volume manufacturing as originally predicted at the 130nm node, which remained dominated by SiO₂ and FSG (Fluorinated Silicate Glass) [5]. This trend continued at the 90nm node where SiO₂ and FSG remained the dominant choices, with first generation carbon-doped oxides (BD-1 from Applied Materials and Coral from Novellus) being adopted for some limited applications.

One of the interesting highlights of the industry efforts to implement low-k dielectric was whether to use a cap layer or not. In the early days, there were concerns that slurries or post-CMP cleaning chemistries might damage the low-k film properties and hence, there was an effort to use a cap layer such as SiO₂, Si₃N₄, etc. While this process ensured no damage to the dielectric layer due to the near inactive character of the cap layer, it also increased the effective k-value of the total stack. Over time, the slurry and post-CMP cleaning chemistry suppliers developed formulations that were compatible with the low-k materials. Therefore, uncapped low-k dielectric films are now routinely used in 90nm and even in some 65nm applications.

At present, the 65nm technology is ramping into production, implemented mostly in 2006, and market intelligence indicates that CDO-based materials are the dominant choice for low-k dielectrics. Almost all modified CDO films are hydrophobic in nature, judging from their characteristic properties as available from their respective manufacturers and/or users. However, they are still not porous, and the effective k-value is >2.5 in most cases. Moreover, even at the 45nm node currently being developed, integration activities are largely focused on extending the 2nd generation modified CDO films, preferably without introducing porosity if it can be avoided.

As the industry moves forward into the 32nm and 22nm nodes, it is expected that devices will require aULK dielectric with k-value < 2.4 [6] in order to achieve the desired performance targets. It is believed that porous materials will be required, and potential integrations are already being developed (see Figure 2). One such film is porous DEMS or PDEMS from Air Products and Chemicals, Inc. (see Figure 3). It is also expected that porous films of any composition will most likely require a very thin capping or sealing layer to prevent unwanted penetration of liquids during CMP and post-CMP cleaning.

**CMP Interactions**

The targets for dishing and erosion on Cu lines continue to decrease with each successive generation of devices. According to the ITRS roadmap, the maximum allowable Cu line thinning in an array is already less than 15nm and is projected to be only 6nm by the 32nm node. Achieving this target consistently in manufacturing will require slurries formulated to the specific materials.
system; pads with excellent surface texture control; and processes with razor-sharp endpoint and/or high selectivity to a stop layer. The CMP process subjects the surface of the wafer to a rather hostile environment with the wafer encountering mechanical forces of both pressure and shear while immersed in an aqueous chemical slurry which usually contains tiny suspended particles. As might be expected, the films deposited on the wafer must be capable of withstanding this environment without suffering undesirable irreversible harm.

Unfortunately, all known ULK materials have a strong trend of lower mechanical strength with lower k-values (see Figure 4) [7]. Typical mechanical failure modes include delamination, cracking, and inelastic deformation. For low-k dielectrics, it was generally sufficient to characterize the materials in terms of modulus, crack propagation velocity, and yield strength. With ULK dielectrics, the introduction of nanopores requires additional metrics such as pore size, pore density, and pore interconnectivity—most of which are very difficult to measure with instrumentation currently available in a fab. As the industry transitions to these materials, the CMP process must accommodate the mechanical fragility of ULK by moving toward lower pressure and lower shear process recipes. These two factors are related through the dynamic coefficient of friction, which is itself related to a large number of factors: platen rotation speed, pad composition, surface texture, pad conditioning parameters, particle size and morphology, solids concentration, slurry chemistry/composition (especially surfactant choice and concentration), among others. While the relationship among these variables is often not linear, it is generally consistent that lower pressure leads to lower shear, thus most copper and barrier polishing recipes are being developed at 2psi and below. This maximum pressure is expected to continue dropping as ULK drives toward lower k-values, which demand larger fractional pore volumes and the accompanying degradations in mechanical strength (Figure 5) [8].

With the focus on mechanical issues with ULK, it is sometimes easy to forget that polishing slurries also contain a mixture of chemical ingredients, such as oxidizers, complexing agents, passivation additives, selectivity modifiers, and surfactants. Slurry developers historically benefited from having dielectric films, such as TEOS or FSG, that were reasonably inert and easy to clean. This is no longer the case with ULK materials, which typically have a strong tendency to absorb water (and other chemicals) from the slurry or at least trap them in any exposed pores. This often results in a higher k-value than the as-deposited film and/or a lower time-dependent dielectric breakdown (TDDB), either of which is problematic for the device. Many of these interactions are also not universal across all ULKs, so chemical formulations in slurries must either strive for a balance of properties compatible with multiple materials, or be reformulated for each specific ULK. Either of these requires additional time and resources to develop.

Development of a CMP process for any of these advanced integrations must be approached as a multi-level, multi-disciplinary project. The properties of the ULK film, the barrier material, the copper deposition technique, annealing cycles, and many other factors will...
influence the CMP process. The situation is made even more difficult by the fact that many of the ULK materials themselves are still being formulated, unlike earlier nodes where at least the dielectric, i.e. FSG or CDO, was locked in at a relatively early stage. This difficulty is compounded by the complexity of developing sophisticated integrations with porous ULKs. In the face of rising costs and shrinking timelines, some companies are choosing to join forces and share the burden across partnerships or informal consortia. The industry is also placing higher expectations on suppliers to provide not only newly formulated materials or consumables, but also more complete data packages showing process responses on test wafers. In many situations, access to process tools and engineering resources can be a major limitation, especially when a fab is running at high utilization rates to meet demand on existing products. Fortunately, some engineering projects lend themselves to being executed by external resources. CMP can be performed on either test wafers or live product prototypes at a properly equipped external facility such as Entrepix, and shipped back to the integration development team for next level processing with minimal risk. This option is being utilized by numerous fabs - including top tier ULK and consumables suppliers - to accelerate project timelines and leverage the focused CMP expertise now available.

**Post-CMP cleaning**

Post-CMP cleaning is an integral part of the CMP process module to clean up the debris and other chemical residues left on wafers during CMP. There are two types of cleaning technology in use: megasonic bath and double-sided scrubber with PVA brushes. Both have advantages and disadvantages and may be employed individually or in combination, as needed, to achieve effective cleaning of the wafers. The megasonic approach is sometimes useful in removing particles from narrow recesses of a polished wafer if the surface features are not completely planar. Brush scrubbers, on the other hand, are particularly useful at dislodging particles that may be physically attracted to the copper surface. It is relatively common to use the combination of both megasonic cleaning and brush scrubbing to give a more robust cleaning process. There are cases of fabs using only one technique, with the more common single method being brush scrubbing. This practice is still possible due to new generation of cleaning chemistries that enable complete removal of particles from the copper surface through chemical and electrochemical means without the need of megasonic energy to physically lift the silica particles off the copper surface.

The technology of using chemistry and electrochemistry to remove particles from a copper surface has become necessary to address the constantly shrinking size of what are considered ‘killer’ defects. In general, this includes any particle greater than the linewidth of the smallest feature, which is now smaller than the particle sizes used in most commercial slurries. Silica particles, for example, will stick to the metal surface by electrostatic bonding if the slurry's pH is acidic. In this case, silica acquires a net positive charge while the surface charge of copper becomes negative. The electrostatic bonding is fairly strong and, traditionally, megasonic energy was needed to lift the particles off the copper surface. With the new generation of acidic post-CMP cleans, the particles are lifted off the copper surface by a very slight etching of underlying copper which is not enough to damage the copper surface topography. In contrast, if an alkaline slurry is used for the final step in the CMP process, the silica becomes negatively charged and floats near the copper surface. It becomes easy to remove these particles, either by an alkaline or acidic cleaning chemistry, as there is no significant particle-surface attraction. Surfactants can also be useful to form a layer around the particles, assisting not only in removing them from wafer surface, but also preventing their redeposition.

Post-CMP cleaning processes must address more than just particle removal. Other killer defects like unwanted metal particles or trace metal ions need to be removed as well, especially at 65nm nodes and below. The new generation of post-CMP cleaning formulations are able to capture such metallic ions more efficiently, leaving a cleaner wafer surface than ever before (see Table 2).

As mentioned earlier, most of the low-k and ULK films are hydrophobic in nature. In order to efficiently clean particles as well as trace metals and organics off the surface of the wafer, it is essential to make the film hydrophilic, at least temporarily, to enable the smooth flow of aqueous cleaning solution followed by rinse water. This is also necessary to avoid leaving water marks. As the following example shows, one of the more efficient ways to do this is to use an appropriate wetting agent in the cleaning formulation to reduce the contact angle from a typical 50 degrees to below 20 degrees. After a normal cleaning process, no water marks are found. Otherwise, if the contact angle...
remains high, water marks are very common, and can also leave behind unwanted high levels of trace metals on the wafer surface.

When the dielectric is made temporarily hydrophilic with a wetting agent, there is often a concern about damaging the dielectric properties, especially since uncapped dielectric film is now in use. The following example shows that for non-porous dielectric films, a well-formulated post-CMP cleaning chemistry does not change the film properties before and after cleaning (see Figure 7).

Even for porous low-k film such as PDEMS, where a cap layer needs to be used, there are concerns about what the impact will be if the cap layer is breached. Experiments performed on uncapped PDEMS ULK suggest that there is a slight shift in k-value and modulus when processed with a standard post-CMP cleaning process. However, a post-cleaning technique was developed to drive out the liquid that penetrates the surface pores of the film. After this step was performed, the PDEMS returned to its normal properties with no apparent residual effects (see Figure 8).

A novel approach to dealing with porous ULK materials in the CMP process module is to delay the formation of the pores until after the entire CMP process module is complete. Several companies are investigating this delayed removal of the porogen as a possible means to not only avoid the liquid penetration issues, but also provide additional mechanical stability for the film stack during polish.

**Future direction**

The future direction for the interconnect module at 32nm and 22nm appears to be nano-porous ULK in a capped integration scheme to minimize the risk of chemical penetration into the material. While some IDMs have adapted uncapped low-k integrations for 65nm, and are pushing similar approaches at 45nm, none of these materials are porous. The issues of water absorption and chemical retention in porous ULK materials appear to be driving most integration teams to include a capping or sealing layer as part of their integration. The cap can also provide a reasonable stopping layer for CMP. The preferred ULK deposition technique appears to be PECVD with either thermal
or ultraviolet porogen release, though spin-on films are still possible if other issues can be resolved. The CMP process is driving toward the lowest possible downforce and lowest possible shear, which requires cooperative development efforts from consumables suppliers, equipment OEMs, and process teams in the fab. Only through this combined effort can processes and materials systems be developed that will meet all required manufacturing metrics for performance, reliability, repeatability and cost per wafer.

<table>
<thead>
<tr>
<th>Dielectric Constant</th>
<th>Hardness (GPa)</th>
<th>Modulus (GPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before treatment</td>
<td>CP72B (20:1)</td>
<td>CP72B (20:1) + post clean process</td>
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Figure 8. CP72 is benign to dielectric network.

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REFERENCES


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