CMP FastForward™

Emerging CMP Applications

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Keynote Panel III

CMP-MIC Conference

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Overview

Questions that must be asked

Categories of Emerging CMP Applications

- **Devices & Technologies**
- **Materials**

Examples

- **Advanced Substrates**
- **MEMS**
- **Direct Wafer Bonding**
- **Multi-Material Application**

Future Challenges

Intro

Keynote Panel Objective:

“Identify new and novel applications for which CMP will be required in the future.”

The range of novel applications is enormous and growing. This can be highlighted from the perspective of a supplier (consumables, equipment, services, your choice) … and identifying the best approach to a potential new application is a bit like playing that familiar game of “20 Questions”.

Why CMP?

Q: Why does this application need CMP?

Typical answers include one or more of …

- Surface needs to be really flat and really smooth
- Too much topography for next process step
- Need to create inlaid material in an etched pattern (aka damascene)

Historical Drivers

The original drivers for CMP in CMOS device fabrication were (and often continue to be) related to issues in other process modules or with the overall integration.

- ***Oxide CMP***
  - **Driver #1: Depth of focus at photo**
    - **Worse as linewidths shrank below 0.35 um**
    - **Worse with additive topography of MLM**
  - **Driver #2: Metal step coverage**
    - **Metal thinning on steep sidewalls**
    - **Topography induced etch effects**
    - **Inconsistent line resistance**
- ***Tungsten CMP***
  - **Preferred alternative to plasma etchback**
  - **Solves severe plug recess from overetch**
  - **Lowers defectivity**
  - **Enables stacked vias**
- ***Shallow Trench Isolation CMP***
  - **LOCOS isolation hit physical limits**
  - **Shrinks below 0.35 um required new isolation**
  - **Original integration used reverse mask etch**
    - **Very sensitive alignment**
    - **Very expensive**
  - **Direct STI CMP required years of slurry innovation and process development**
- ***Copper CMP***
  - **Driven by lack of acceptable Cu metal etch**
  - **Planarity is key to consistent line resistance**
  - **Introduction of low-k and ULK dielectric complicates an already difficult materials system**

Devices and Technologies

Q: What device or technology is involved?

- ***Advanced Substrates***
  - Strained layer epi
  - SOI
  - Wide bandgap materials
  - Infrared detector substrates
- ***MEMS***
  - Structural components (often polysilicon)
  - Sacrificial spacers (oxides – dissolved later)
  - Separation layer (MEMS-first or MEMS-last)
- ***Packaging and 3D***
  - Through-Silicon Vias (TSV) for memory, image sensors, communications, etc.
  - Interposers for double-sided flip chip
  - Ultrathin grind / stress relief polish
- ***Direct Wafer Bonding***
  - Anything to almost anything else
- ***Integrated Optics***
  - Grating structures
  - Embedded waveguides
  - Integrated optical transducers/modulators
- ***Microelectronics***
  - New materials for integration with CMOS
  - Phase change and other exotic memories
  - Power devices
  - Mixed signal and RF devices
  - High performance discrete components
- ***Other***
  - Surface reference standards
  - Magnetic shielding or active components

Materials Questions

Q: What material needs to be polished?

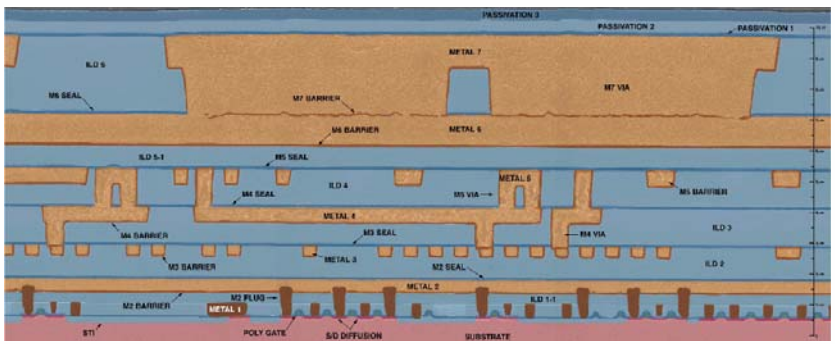
Additional questions may be triggered …

- Bulk or thin film?
- How many materials need to be coplanar?
- Is there a stop layer? If so, what?

CMP Evolution in CMOS

1995	2001	2008
Glass (oxide)	Glass (oxide)	Glass (oxide)
Tungsten	Tungsten	Tungsten
	Shallow Trench	Shallow Trench
	Copper	Copper
	Polysilicon	Polysilicon
		Low k
		Capped Ultra Low k
		Metal Gates
		Gate Insulators
		High k Dielectrics
		Ir & Pt Electrodes
		SOI / Strained Layers

Future Trend?



Materials Viable for CMP

CMP has been developed or is being developed for all of the following:

Polymers	Metals	Minerals
Low-k and ULK	Copper	Oxides
Polyimides	Tungsten	Nitrides
Polyurethanes	Aluminum	Si, Polysilicon
SU8	Tantalum	Ge and SiGe
BCB	Titanium	III-V (GaAs,GaN,InP,etc.)
Polycarbonate	Ruthenium	II-VI (CdTe,HgCdTe,etc.)
Hardened Photoresist	NiP	SiC, SiOC
	NiFe & magnetics	Carbon Nano Tubes
	Pt, Ir, and other nobles	Phase Change Materials

Note similarity to one of the classic 20 Questions …
"Animal, vegetable or mineral?"

Dimensional Questions

Comparable to … “Is it bigger than a bread box?”

Typical questions for bulk substrates

- Wafer size? (Don’t laugh!)
- Incoming and target thickness?
- TTV, bow, warp requirements?
- Surface roughness: Incoming and target?

Typical questions for thin film applications

- Film stack composition and layer thicknesses?
- Incoming topography and required after polish?
- Feature sizes and pattern density? (dummy fill?)
- Thickness targets AND tolerances? (including uniformity requirements)

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Other relevant questions

Questions related to likelihood of 1st pass success:

- Any observed film stress, mechanical integrity or delamination issues?
- Any known aqueous chemical incompatibility?
- Sensitivities to surface contaminants?
- Number of substrates available for CMP work?
- How many blanket film test wafers of each material?

Now what ??

After asking a whole lot of questions to understand the scope of a new CMP application …

… the time comes to brainstorm the closest known process then put together a development plan and get some answers !!

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Intro to Examples

- ***Advanced Substrates***
  - Strained layer epi
  - SOI
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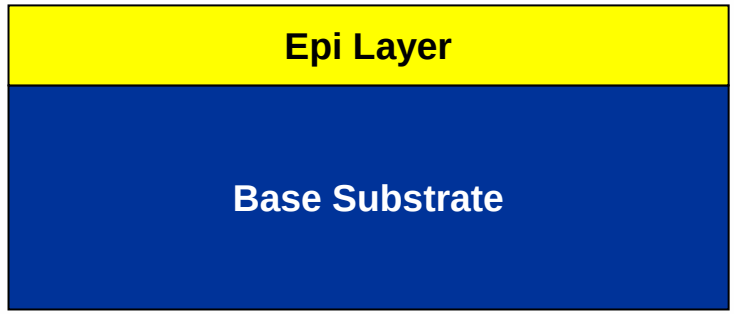
Advanced Substrates

Typical Materials

- SOI
- Strained Layer SiGe
- III-V or II-VI or composites



Key Aspects of the Application

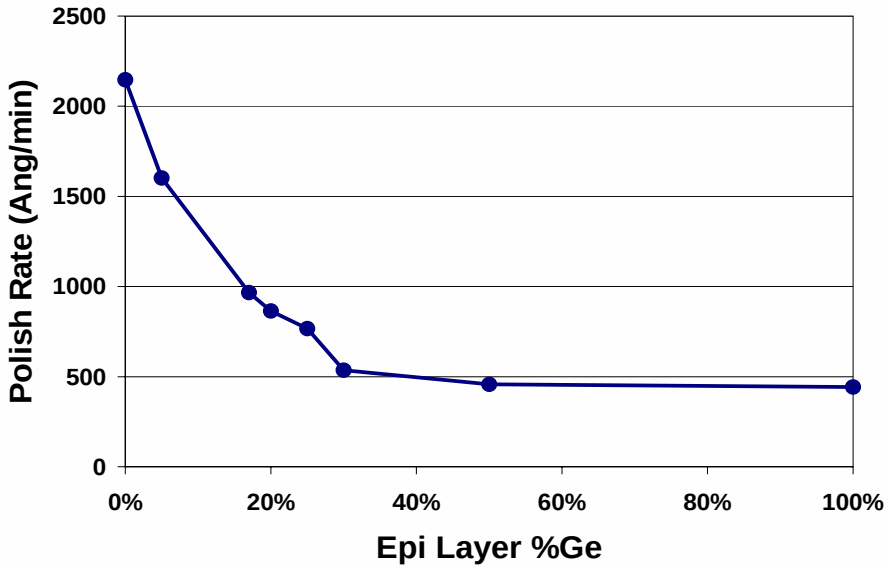
- Strained layer technology being used to increase carrier mobility in Si devices
- Heteroexpitaxy of mismatched materials seeing growing # of applications
  - Usually creates huge density of threading dislocations and other issues
  - Extremely high roughness needs polishing to be device-ready
  - Some materials (esp. II-IV blends) difficult to polish w/o anisotropic etching
- Cleaning of polished surfaces is often difficult (Ge is etched by NH4OH)

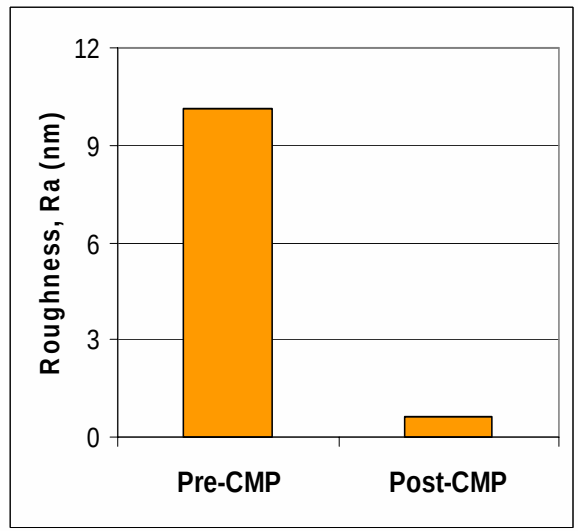
Example: SiGe Epi

Process Factors:

- Standard Si process left Ra too high
- Post-CMP clean had to be developed
- Composition varied widely

Metric	Incoming Value	Target	Actual
Surface Roughness, Ra	>10 nm	<1 nm	0.2-1.4 nm
Removal Rate	n/a	>500 A/min	480-1600 A/min
Total Mtrl Removal	n/a	0.25-0.75 um	Within 5%





MEMS Applications

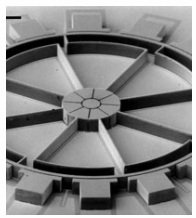
Typical Devices:

- Accelerometers
- Torque sensors
- Optical devices
- Microfluidic processors

Typical Materials

- Undoped oxides (TEOS, silane, etc.)
- Doped oxides (PSG, BPSG, etc.)
- Polysilicon
- Some metals (specialized apps)

Key Aspects of the Application



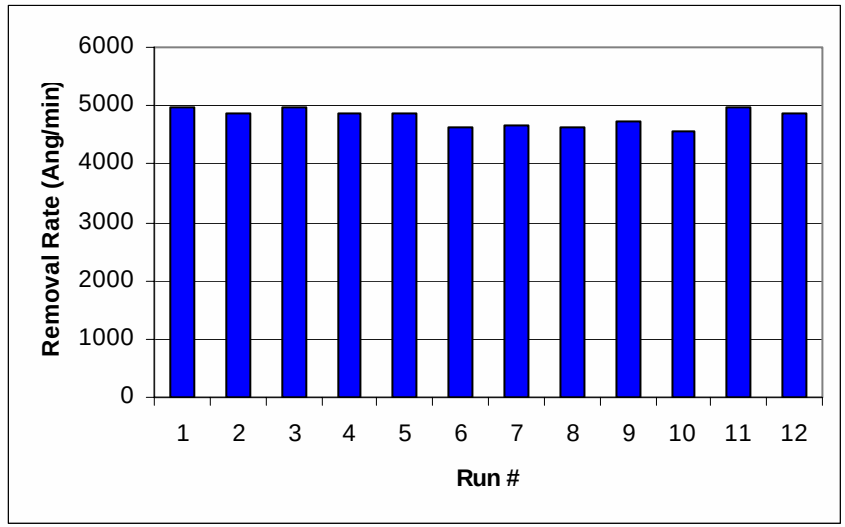
- Materials and core processes generally adapted from CMOS fabrication
- CMP is an enabling technology for many designs
- Thicknesses and step heights substantially larger than typical of CMOS
- Lengthy polish times challenge process stability & consumables lifetime

Photos downloaded from web sites, including Sandia National Lab

Example: MEMS Last

Critical Concerns:

- Minimize oxide deposition
- Incoming topography 2.8 um
- Final topography must be < 0.4 um
- Smooth – No sharp corners anywhere
- Batch to batch consistency



Key Process Metrics & Constraints

Metric	Incoming Value	Target	Actual
Oxide film thickness	6.5 um	3.0 um	3.02 um
Topography (Step Height)	2.8 um	< 0.4 um	0.2 um
Removal Rate (um/min)	n/a	0.5	0.488

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Direct Wafer Bonding

Material Stack	Incoming Ra (A)	Post-CMP Ra (A)
TEOS on Silicon	7	3
TEOS on SiC	72	7
TEOS on Polysilicon	87	7
TEOS on AlN	187	11
TEOS on Metal	332	8

Example #1: TEOS on X

- Oxide surfaces tend to bond well when polished to sufficiently low Ra
- Incoming roughness driven by surface prep of underlying material
- Sufficient oxide thickness must be deposited to remove over 2x initial peak-to-valley roughness

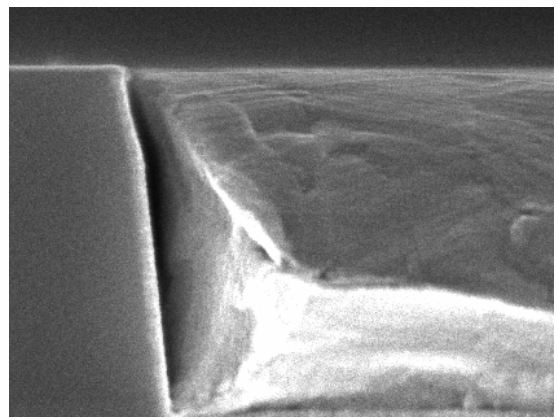
Example #2: Inlaid Cu in TEOS

- Incoming topography >2.5 kA
- Goal of <200 A total topography

POST-CMP TOPOGRAPHY ACHIEVED

70-90 Angstroms

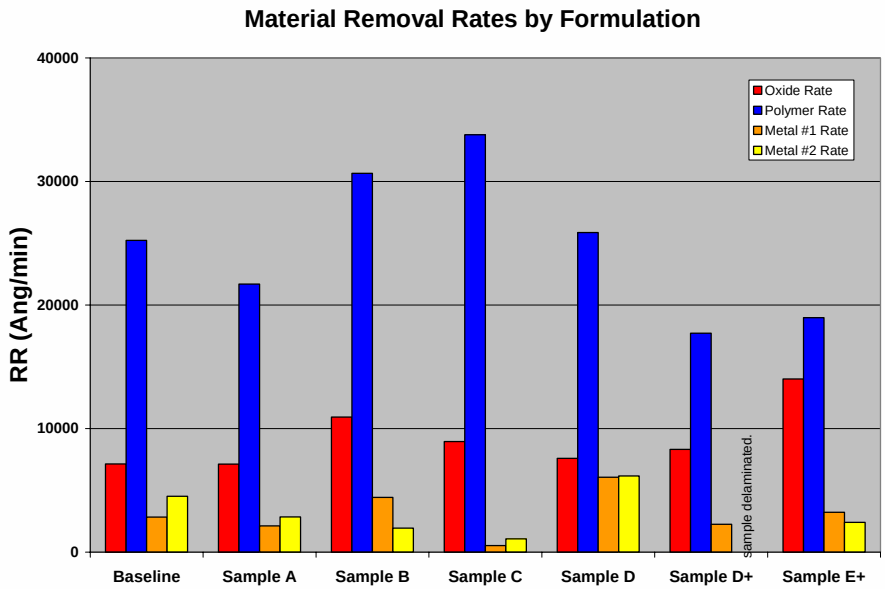
→ Flat across Feature



Multiple Materials

Multiple Materials

- Final surface is comprised of oxide, polymer, and two different metals
- Goals of CMP process:
  - High rate on oxide and polymer
  - Low Ra on all materials
  - Planar surface across all mtrls
- Project focused around new slurry formulations



Data		Removal Rate				Roughness (Ra)			
Run Order	Slurry	Oxide Rate	Polymer Rate	Metal #1 Rate	Metal #2 Rate	Oxide Ra (Ang)	Polymer Ra (Ang)	Metal #1 Ra (Ang)	Metal #2 Ra (Ang)
1	Baseline	7129	25233	2834	4521	6	12	n/a	5
2	Sample A	7121	21688	2118	2846	6	6	13	14
3	Sample B	10918	30655	4431	1942	14	6	37	7
4	Sample C	8940	33784	521	1071	16	19	672	7
5	Sample D	7595	25859	6060	6163	5	14	48	11
6	Sample D+	8307	17726	2248	n/a	5	6	26	n/a
7	Sample E+	14004	18977	3225	2411	5	9	13	11

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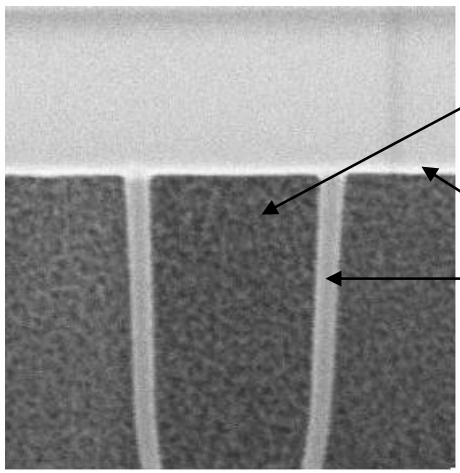
Microelectronics

Example Parameter	Value or Description
Top layer material	Polysilicon
Bottom layer material	Oxide (undoped)
PolySi removal rate	4100 Ang/min
Selectivity (PolySi:Oxide)	>100 : 1
Planarization Efficiency	> 99%

Example: Polysilicon on Oxide

- **Pattern cut into Si wafer**
- **Deposit thin oxide layer then grow polysilicon onto entire surface**
- **Goal of CMP process is to stop on thin oxide without breaking through and planarize across all inlaid features**
- **Multiple pads and slurries screened**
- **Successfully demonstrated materials integration for future design inputs**



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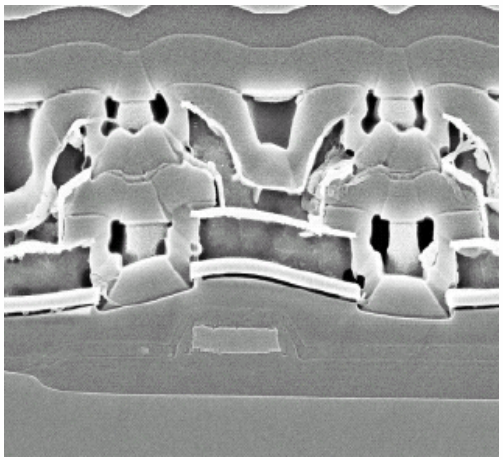
CMP Expectations

- QUALITY
  - Reliability of finished devices can not be compromised (Hippocratic oath)
  - Final surface must meet required (not necessarily desired) specs
  - Process repeatability and yield have to be acceptable
- SPEED
  - Develop process quickly and with fewest possible number of iterations
  - Leverage existing process and materials knowledge as much as possible
- COST
  - Development cost varies widely depending on material and device
  - Process optimization should include all relevant factors, including cost/wfr

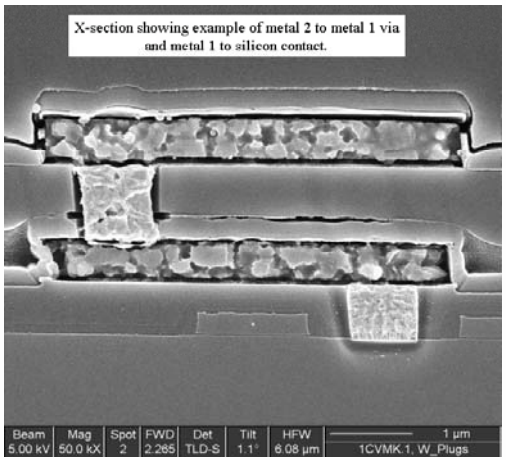
Parting Perspective

Emerging technology often starts with something simple … but then …

Traditional device (no CMP)

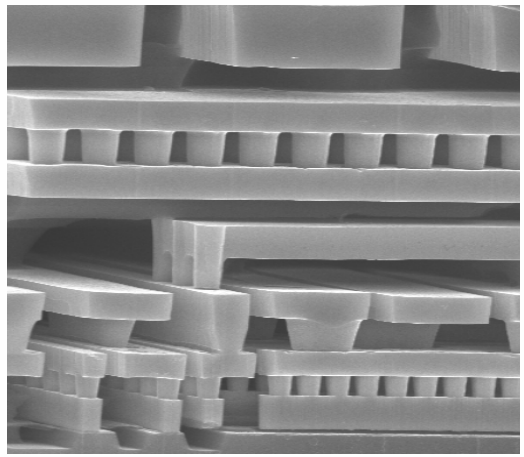


New device (4 CMP steps)



Pictures courtesy of Medtronic, Inc.

Advanced Device (12 CMP steps)



Picture courtesy of Freescale Semiconductor, Inc.

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Thank you

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