CMP For Direct Wafer Bonding of Hermetically Sealed Cavity Structures

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Outline

Introduction and Background

CMP Development for Direct Wafer Bonding

Post-CMP Cleaning Optimization

Pull Strength Testing and Hermiticity Results

Conclusions
• Direct Wafer Bonding (DWB)
  – Multiple types now available
  – Surface preparation often includes CMP
  – Cleaning steps are critical to ultimate DWB success
  – Anneal is necessary to strengthen bonds
Types of Si DWB

Hydrophobic vs. Hydrophilic Activation

**Hydrophobic Activation**
- Dilute HF dip followed by room temperature bonding.
- The surfaces are oxide free and terminated with hydrogen and fluorine atoms.
- The surfaces are weakly bonded together by hydrogen bonds before annealing.
- After annealing, a pure, electrically and thermally conductive Si-Si bond remains.
- The activation temperatures for hydrophilic bonding are lower than hydrophobic because hydrogen gas is easier to remove than water molecules.

**Hydrophilic Activation**
- After an RCA clean or SC clean (H₂O:H₂SO₄:NH₄OH) and dry at 90 °C, the native oxide on each wafer is terminated with OH groups.
- These groups attract water so the surface is hydrophilic.
- The dried wafers are brought into contact at room temperature and the bond initiated at a point.
- The wafers are heated to anneal the bond.
- The heat drives the water molecules out, leaving behind a Si-O-Si bond, which is very strong.

Source: Kim and Najafi, University of Michigan, 2007
3D Packaging Apps

1. "3D-WLP" Era
   - Vias: > 50 μm
   - Holes: < 50
   - t: > 200 μm

2. "3D TSV Stack" Era
   - Vias: > 20 μm
   - Holes: < 1000
   - t: 50 μm

3. "3D Fusion" Era
   - Vias: 10-30 μm
   - Holes: > 100
   - t: < 50 μm

4. "3D Logic-SiP" Era
   - Embedded memory
   - Vias: 5-20 μm
   - Holes: > 100K
   - t: < 100 μm

5. Ultimate 3D IC
Hermetic Cavities

- Material constraints
- Size constraints
- Medical applications
  - Implantable parts and components
  - Must survive hostile environment >7 years
  - Material constraints
- Why is this so different than 3D ??
Why is CMP so critical?

- Highlight surface preparation importance
- Key parameters: Flat, smooth, clean
Guideposts for DWB

- **Surface Roughness (Ra)**
  - $< 0.5 \text{ nm}$
  - $0.5 – 1.0 \text{ nm}$
  - $> 2.0 \text{ nm}$
  - Good ……. Usually ok ….. Poor

- **Flatness or topography**
  - No “bumps” sticking up from surface
  - Indents or cavities ok (preferably sharp corners)

- **Surface cleanliness**
  - Must be very clean and particle free
  - NO hydrocarbons

- **Materials**
  - Strongest bond is generally same-same material
  - Most common are oxide-oxide and Si-Si
• Zoom in on CMP process development
• Assumes fundamentals of pad/slurry research are already done by suppliers
• Test wafer availability and quality often impact timeline, validity of results, etc.
• Initial process DOE’s generally focus on removal rate and gross surface quality

Optimization stages can be interchanged or executed in parallel

• Planarity can mean step height, dishing, erosion, roughness, etc. depending on the material and intended application
• Failure at any stage usually means backing up at least one stage to try again
A proven approach to successfully developing new CMP processes

- Screening Tests
- Optimization
- Repeatability
- Marathon
• Included 3 types of substrates
  – Silicon wafers with grown thermal oxide layers
  – Silicon wafers with deposited TEOS films
  – Borofloat 33 glass (clear)

• Initial work performed on bare substrates and blanket film wafers to understand materials independent of pattern effects
**Test Inputs**
- Thermal oxide films
- IPEC 472 polisher
- Klebosol silica slurry
- IC1000 on Suba IV pad stack
- Diamond pad conditioner

**Outcome**
- Two pressures screened
- Linear function of polish time
- Surface roughness excellent at all settings (Ra <1 nm)
 CMP – Borofloat 33 Glass

Test Inputs
- Substrates of Borofloat 33
- IPEC 472 polisher
- Klebosol silica slurry
- IC1000 on Suba IV pad stack
- Diamond pad conditioner

Outcome
- Same two pressures screened
- Removal rate ~50% faster than same process on thermal oxide
- Multiple wafers per data point shows excellent repeatability
CMP Issues with clear Borofloat 33 substrates

- **Wafer metrology**
  - Unable to use thin film metrology on clear wafers
  - Adapted “weight loss” technique for control

- **Post-CMP clean**
  - First attempts with OnTrak double-sided scrubber failed due to sensors not “seeing” clear wafers
  - Developed modified sensor kits that now allow the OnTrak DSS to process all wafers w/o error
OnTrak Systems

Series II Classic or CE

Synergy

Synergy Integra

Load Station  Dual Brush Module  Spin Station  Unload Handler  User Interface

Chemical Dispense Manifold (Drip)  PVA Brush  Polyurethane Rollers

97.29 inches  28.56 inches
OnTrak Sensor Issues

- The system utilizes wafer sensors for feedback and control.
- Typical config includes through beam sensing to detect the presence or passage of opaque substrates.
- Clear substrates are not detected by through beam sensors nor standard capacitive sensors.
- In dry environments, reflective sensors are a good solution.
- Post cmp cleaning environment involves liquid sprays, highly polished metals and plastic surfaces, and other reflective surfaces which generate “noise” to the typical reflective sensor.
- Tuning a standard reflective sensor to detect only the substrate and not the liquid overspray or materials was ineffective.
Sensor Locations

Multiple Sensors:
- Load station
- Brush box #1
- Brush box #2
- Transfer carriage
- Spin station
- Unload station
New sensor types employed for clear wafers

1) Definite Reflective Sensors
   • Allows detection of a surface at a specific point (+\-.02”).
   • Mounted near to the product surface (1-2” preferred).
   • Uses a digital amplifier to suppress “noise” generated by background surfaces or water droplets.

2) Retro-reflective Sensor
   • Enables longer distance sensing
   • Amplifies attenuation in received light even as it passes through a clear surface.
Definite Reflective Sensors

The most intense received light is reflected from the surface of the product. Other received light can be tuned out using the amplifier.
Retro-reflective Sensor

When system constraints require longer distance sensing a polarized surface mounted opposite the sensor assists in amplifying any attenuation in light caused by presence of the substrate.
Pull Test Procedure

- Only performed on unpatterned bonded pairs (no device cavities) to test uniform bond strength
- Dicing saw used to cut 0.25”x0.25” samples
- Posts bonded to each side with epoxy
- Alliance RT/10 MTS Tensile Tester
- Three common failure modes
  - Bulk Fracture (FR)
  - Adhesive Failure (AF)
  - Bond Failure (BF)
Edge chips may have contributed to some Si bulk fracture failures.
Bulk Fracture Failure
Bond Interface Failure
### Table I. PULL TEST DATA (PSI) - BOROFLOAT GLASS WITH VARIOUS CMP

<table>
<thead>
<tr>
<th>Sample</th>
<th>Silicon 2.0um CMP</th>
<th>Borofloat 3um CMP</th>
<th>Borofloat 1 um CMP</th>
<th>Borofloat 0.45 um CMP</th>
<th>Borofloat 0.15 um CMP</th>
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<tr>
<td>1</td>
<td>1672 (FR)</td>
<td>2177 (FR)</td>
<td>2287 (AF)</td>
<td>1387 (AF)</td>
<td>1303 (AF)</td>
</tr>
<tr>
<td>2</td>
<td>1928 (AF)</td>
<td>2679 (FR)</td>
<td>2495 (AF)</td>
<td>3033 (FR)</td>
<td>3046 (AF)</td>
</tr>
<tr>
<td>3</td>
<td>2493 (FR)</td>
<td>2465 (FR)</td>
<td>3058 (L)</td>
<td>3058 (L)</td>
<td>2802 (AF)</td>
</tr>
<tr>
<td>4</td>
<td>3059 (L)</td>
<td>2137 (AF)</td>
<td>3059 (L)</td>
<td>3058 (FR)</td>
<td>3058 (L)</td>
</tr>
<tr>
<td>5</td>
<td>3059 (L)</td>
<td>2693 (FR)</td>
<td>2473 (AF)</td>
<td>3041 (FR)</td>
<td>297 (BF)</td>
</tr>
<tr>
<td>6</td>
<td>1286 (FR)</td>
<td>2380 (FR)</td>
<td>1433 (AF)</td>
<td>3058 (L)</td>
<td>2820 (AF)</td>
</tr>
<tr>
<td>7</td>
<td>1672 (FR)</td>
<td></td>
<td>2619 (AF)</td>
<td>2752 (AF)</td>
<td>2302 (BF)</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>857 (AF)</td>
<td>2452 (AF)</td>
<td>2714 (BF)</td>
<td></td>
</tr>
<tr>
<td>Avg/Std</td>
<td>2430 +/- 265</td>
<td>2285 +/- 770</td>
<td>2729 +/- 584</td>
<td>2292 +/- 988</td>
<td></td>
</tr>
</tbody>
</table>
Pull Test Implications

• Borofloat 33 wafers required at least some amount of CMP to successfully pre-bond to SiO2 at room temperature.

• Borofloat 33 wafers that were polished to remove at least 1um of material had fewer bond failures during pull tests.

• For the highest removal group (3um), bulk fracture of the Borofloat 33 was the most common pull test failure.
  – Possible residual stress from TCE mismatch during anneal
  – Possible inclusions or defects in the glass
  – Lower intrinsic fracture strength than single crystal silicon
Test Inputs
- Cavities patterned in Si wafers than coated in oxide
- IPEC 472 polisher
- Klebosol silica slurry
- IC1000 on Suba IV pad stack
- Diamond pad conditioner

Outcome
- Range of processes studied for impact on cavity edges
- Relatively linear response across range of CMP index (confirms Prestonian behavior)
- High pressure settings showed more edge rounding
Sealed Cavity

Excellent bond – no evidence of separation along interface

Cavities were fabricated across a range of CMP processes and total removal using both Borofloat 33 cap wafers and Si cap wafers with an oxide film.
He Leak Rate Tests

- Cavities singulated and checked for integrity
- Placed in pressurized He chamber for >48 hrs
- Generalized leak rate test method
  - Establish initial baseline (empty chamber pump cycles)
  - Measure two data points per sample
  - Repeat baseline at end of test
  - No sample is allowed out of pressurized He chamber for more than 2 hours
- Test method compatible with MIL-STD-883
Cavities in Si with SiO2 on Si wafer cap

Observations
- Stable baseline leak rate for empty chamber < 1E-12
- Pink line is calculated threshold per XXXX equation (well below MIL-STD-883)
- Each sample was tested twice in succession for repeatability
- Chamber returned to baseline

Summary
- One cavity failed
- One cavity was borderline
- Twenty-four (24) cavities passed with substantial margin
Observations

- Stable baseline leak rate for empty chamber < 1E-12
- Same size cavities as previous
- Each sample was tested twice in succession for repeatability
- Chamber returned to baseline

Summary

- 100x higher leak rate than cavities capped with Si+SiO2
- One cavity passed (unexpected result given consistency of other samples in dataset)
- Eleven (11) cavities failed to this rigid standard (may still pass MIL-STD-883)

Interim conclusion: Borofloat glass is more permeable than SiO2 on Si
Summary

- CMP removal rate is controllable over reasonable range of settings for both SiO2 and Borofloat 33
- Clear wafers require modification of the sensors in an OnTrak DSS-200 scrubber
- Hermetically sealed cavities can be fabricated using CMP and direct wafer bonding.
- Bond strength is improved when both surfaces are polished and properly cleaned.
- Hermeticity (cavity leak rate) is improved by using an oxidized Si cap wafer compared to borofloat glass
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