

New Technology Trends: Expand & Extend



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Semiconductor Market History

Market Segments

Future Direction: Expand and Extend

Author's Note



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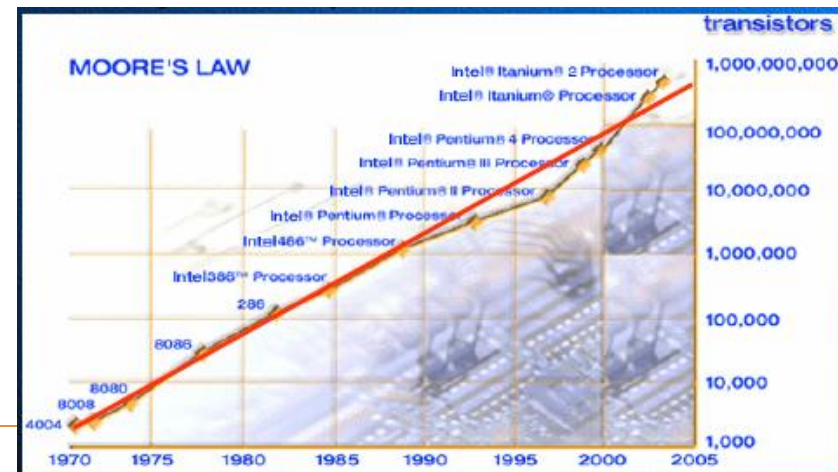
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Your mileage may vary.

Industry Trends

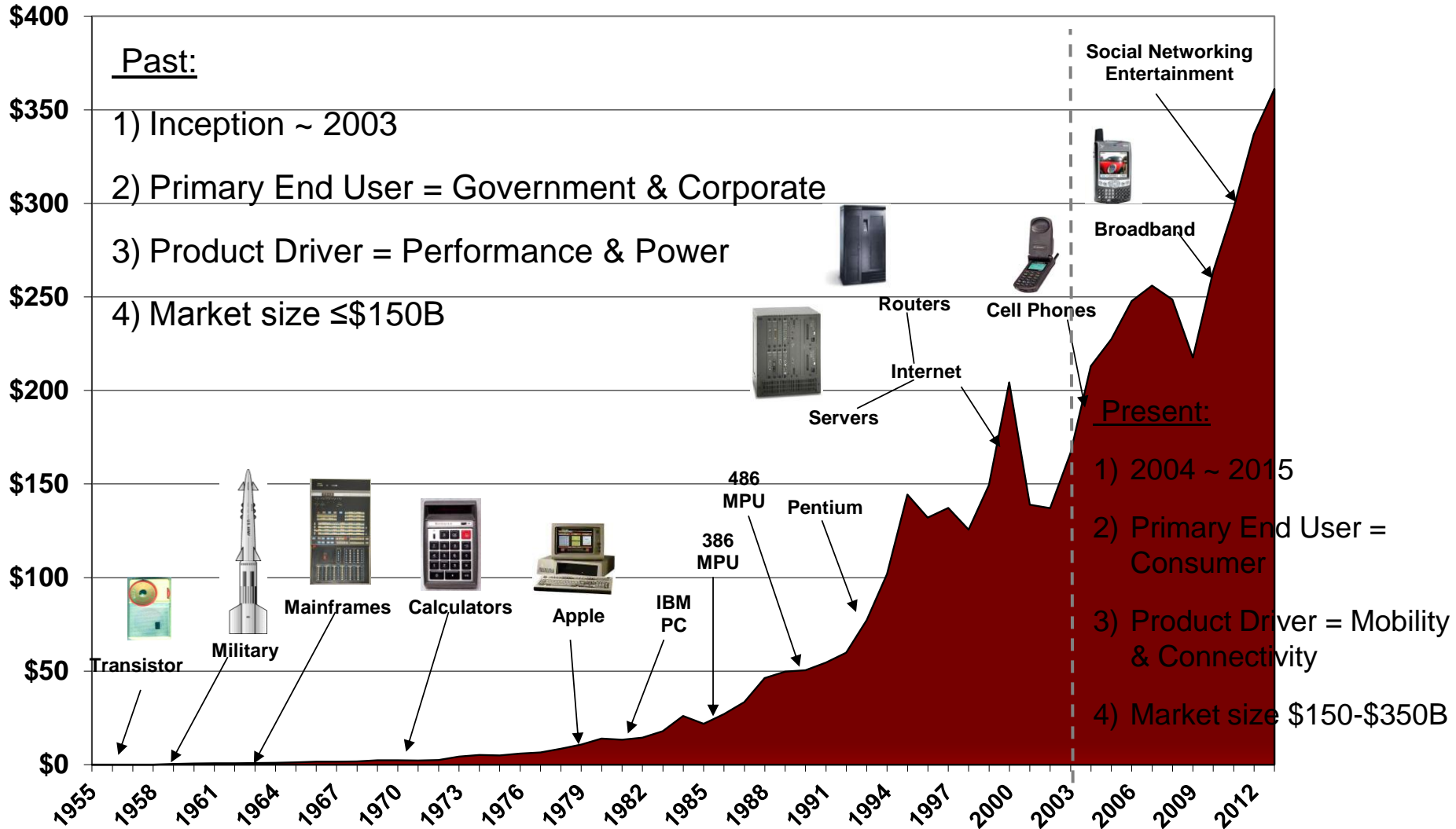


- What drives decisions in the semiconductor mfg? **SPEED and COST!**
 - New products must be ready on time for market launch
 - Long term efficiency improves competitive strength
- Moore's Law dominated the CMOS industry for >40 years
 - Not affected by cycles, markets, analysts, or the economy
- Photolithography and CMP are two critical process technologies to continue both cost and performance improvements
 - Photolithography enables SHRINKS
 - CMP enables more complex STACKS
- Trend still holds for certain industry segments, but many companies are choosing to pursue other paths



Source: Intel Corporation

Semiconductor Market



Source: SIA/WSTS and Semico Research Corp.

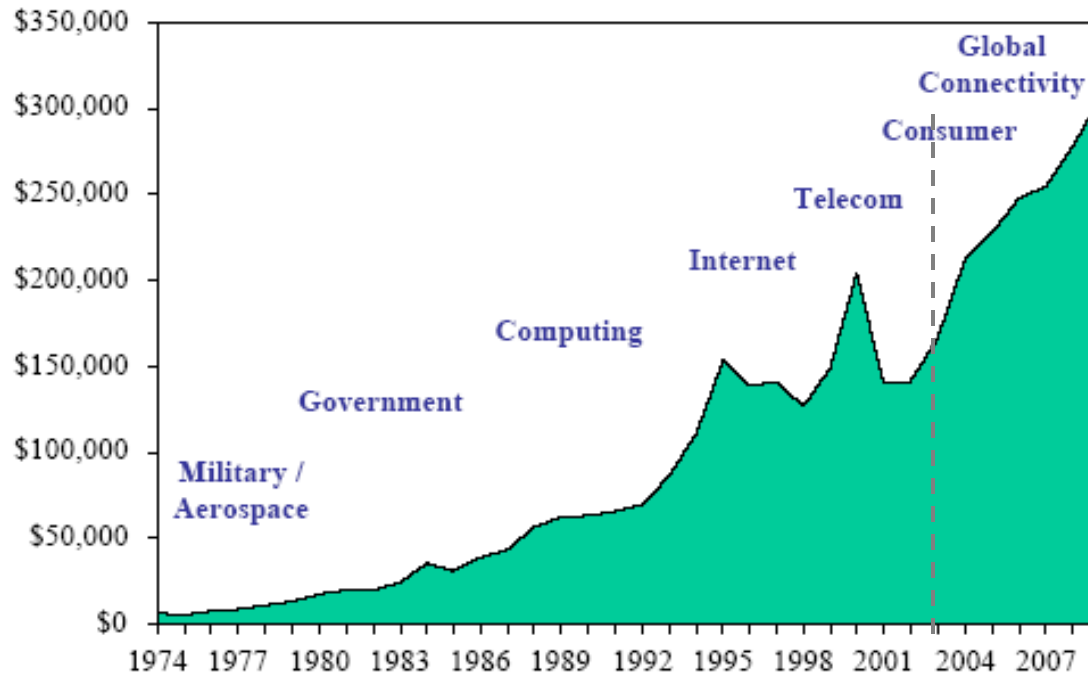
Primary Drivers



Growth Drivers

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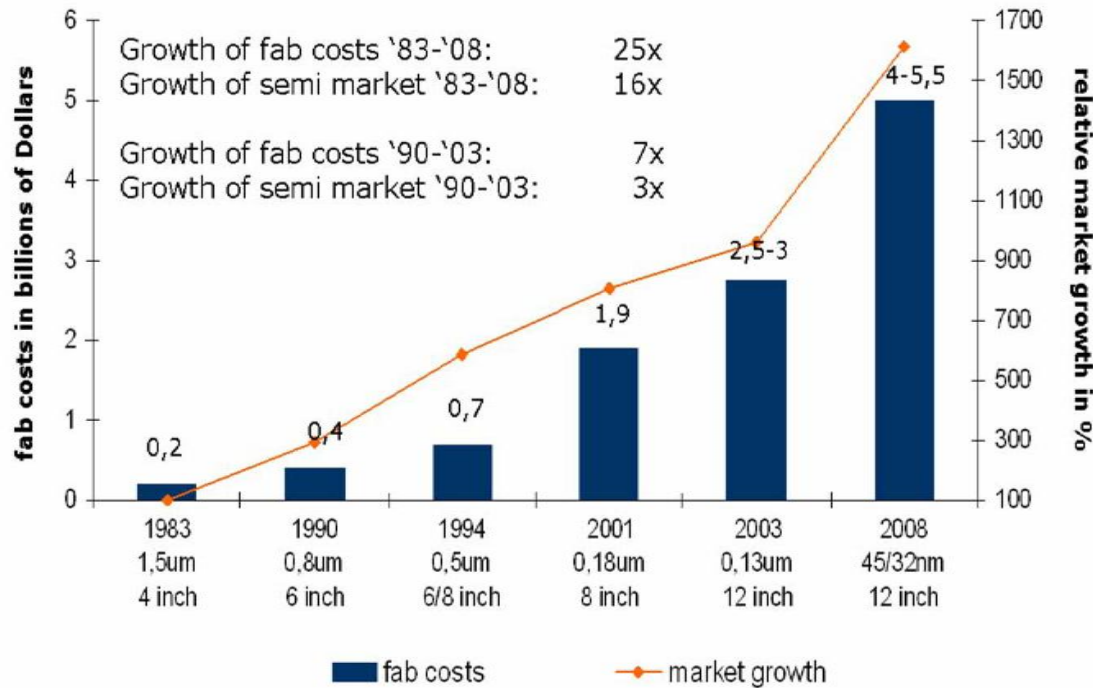
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3

Wafer Fab Investment



Fab costs vs. market growth



Source: Semico Research Corp

EE Times Asia

TSMC preps for \$26B fab

Posted: 16 Dec 2011

Central Taiwan Science Park in Taichung, Taiwan has appropriated a 50-hectare lot for TSMC to build a 450mm wafer fab at a projected cost of around \$26 billion (more than NT800 billion), or nearly three times the cost of TSMC's Fab 15 Gigafab currently being built on the science park.

Technology Nodes



- Historical progression for >20 years
0.5 um → 0.35 → 0.25 → 0.18 → 0.15 → 90 nm → 65 nm → etc.
- Devices, equipment platforms, even entire fabs were identified by their “target node”
- Industry language referenced the expectations
Leading edge – mainstream – trailing edge
Early adopters – fast followers – late stage
Etc.

Still applies to some segments of CMOS devices

But no longer universal terminology.

Industry Segments

Particularly from a CMP perspective



- Segment I – More Moore
 - Wafer sizes: 300mm & likely 450mm
 - Technology nodes: 32nm, 25nm and below
 - Materials: high k, metal gates, ULK, advanced barriers, etc.
- Segment II – More than Moore (New Mainstream)
 - Wafer sizes: 300mm (some), 200mm & 150mm
 - Technology nodes: 90nm to 350nm and above
 - Materials for CMP: oxides, tungsten, etc.
- Segment III – More than Moore (Emerging)
 - Wafer sizes: 200mm, 150mm, 100mm and smaller
 - Technology nodes: various
 - Materials: wide range of metals, oxides, polymers, and more
 - MEMS, nanotechnology, SiC, GaN, optics, etc.

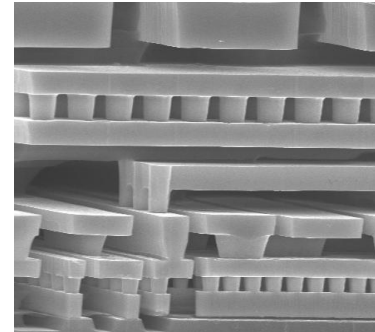
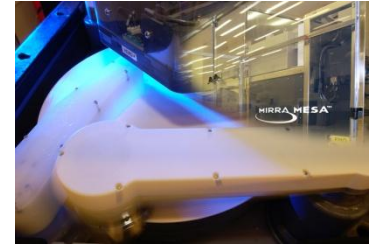


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Segment I More Moore



Financial Factors and Trends Across 3 Industry Segments

| Financial Factor | More Moore | | New Mainstream | | Emerging | |
|-----------------------------|------------|-----------|----------------|-----------|----------|-----------|
| | Level | Direction | Level | Direction | Level | Direction |
| Average Annual Capital | High | ↑ | | | | |
| Technology R&D | High | ↑ | | | | |
| Manufacturing Cost/chip | High | ↓ | | | | |
| Volume | High | - | | | | |
| Average Selling Price (ASP) | High | ↓ | | | | |

Moore's Law

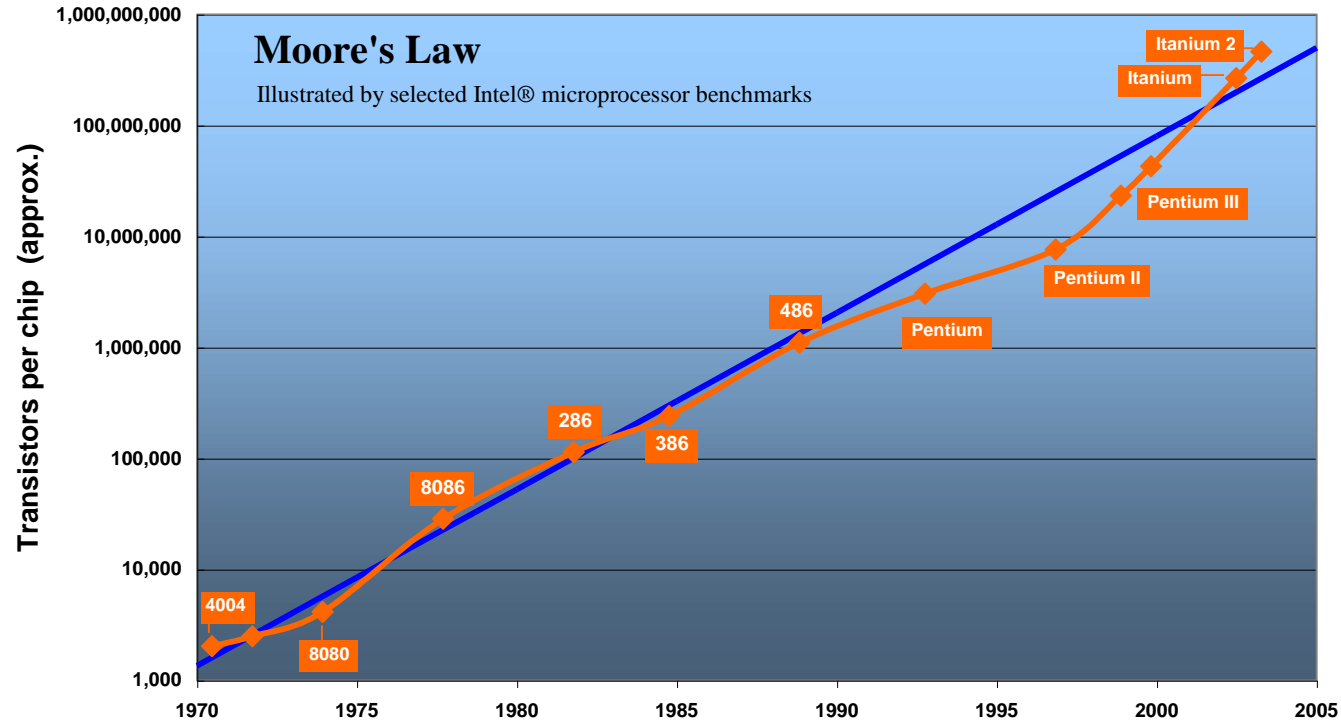


Microprocessor transistors per chip have increased by over 5 orders of magnitude in 40 years.

Current generation chips have more than 1.7 billion transistors

Photo and CMP are 2 critical processes required to stay on trend line:

- Photo → SHRINKS
- CMP → STACKS



Moore's Law has not been derailed by industry cycles, technology hurdles, or the economy ... but it does not really apply to every semiconductor company

Segment I Key Points



- Typical companies: microprocessor and memory makers, large-scale foundries
- Willing to spend capital on new fab construction (300 mm and soon 450 mm)
- Willing to adapt new materials or processes as needed to achieve performance
- Designs AND process technology both change at a rapid pace
- Design focus = performance
- Process focus = speed at acceptable yield

Segment II New Mainstream



Financial Factors and Trends Across 3 Industry Segments

| Financial Factor | More Moore | | New Mainstream | | Emerging | |
|-----------------------------|------------|-----------|----------------|-----------|----------|-----------|
| | Level | Direction | Level | Direction | Level | Direction |
| Average Annual Capital | High | ↑ | Moderate | ↓↓ | | |
| Technology R&D | High | ↑ | Moderate | ↓ | | |
| Manufacturing Cost/chip | High | ↓ | Moderate | ↓↓ | | |
| Volume | High | - | High | ↑ | | |
| Average Selling Price (ASP) | High | ↓ | Low | - | | |

Segment II Key Points



- Wide range of companies and products including digital, analog, mixed signal, power, etc.
- Adapting to a world of flat or falling ASP's
- Cost factors and yield becoming MUCH more important than technology factors
- Some devices enjoy long lifecycles (but not all)
- Designs may change rapidly, but process technology intentionally being held much more stable
- Design focus = features and simplicity
- Process focus = cost and maximizing yield

Segment III Emerging Technology



Financial Factors and Trends Across 3 Industry Segments

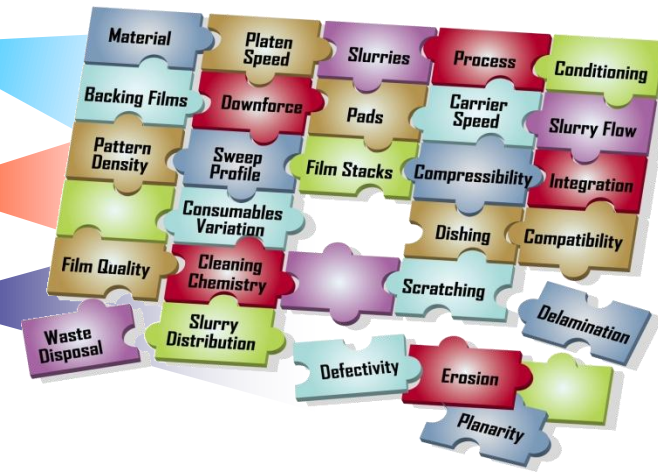
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| | Level | Direction | Level | Direction | Level | Direction |
| Average Annual Capital | High | ↑ | Moderate | ↓↓ | Low | - |
| Technology R&D | High | ↑ | Moderate | ↓ | High | ↓ |
| Manufacturing Cost/chip | High | ↓ | Moderate | ↓↓ | High | ↓ |
| Volume | High | - | High | ↑ | Low | ↑↑ |
| Average Selling Price (ASP) | High | ↓ | Low | - | High | ↓ |

Emerging CMP



| 1995 - Qty ≤ 2 | 2001 - Qty ≤ 5 | 2011 - Qty ≥ 40 | | |
|----------------|-----------------|----------------------|-------------------|---|
| CMOS | CMOS | CMOS | New Apps | Substrate/Epi |
| Oxide | Oxide | Oxide | MEMS | GaAs & AlGaAs |
| Tungsten | Tungsten | Tungsten | Nanodevices | poly-AlN & GaN |
| | Cu (Ta barrier) | Cu (Ta barrier) | Direct Wafer Bond | InP & InGaP |
| | Shallow Trench | Shallow Trench | Noble Metals | CdTe & HgCdTe |
| | Polysilicon | Polysilicon | Through Si Vias | Ge & SiGe |
| | | Low k | 3D Packaging | SiC |
| | | Capped Ultra Low k | Ultra Thin Wafers | Diamond & DLC |
| | | Metal Gates | NiFe & NiFeCo | Si and SOI |
| | | Gate Insulators | Al & Stainless | Lithium Niobate |
| | | High k Dielectrics | Detector Arrays | Quartz & Glass |
| | | Ir & Pt Electrodes | Polymers | Titanium |
| | | Novel barrier metals | Magnetics | Sapphire |
| | | | Integrated Optics | entrepix <small>YOUR CMP PARTNER</small> |

36+ highly complex puzzles
CMP JIGSAW PUZZLE



- Early stage prototype development
- Integration and process optimization
- Qualification and transition to manufacturing
- Yield improvements and cost reductions

Growth in Applications



CMP is still evolving for CMOS applications ...
And many newer applications are now also being developed beyond “traditional” CMP.

- ***MEMS***

- Oxides (doped or undoped)
- Polysilicon (usually structural)
- Nitrides and oxynitrides
- Separation layer (MEMS-first or MEMS-last)
- Metals (esp. for reflective surfaces)

- ***Advanced Substrates***

- Strained layer epi substrates
- Custom III-IV and II-IV epi layers
- SOI
- GaN, GaP, SiC, etc.
- Various surfaces for direct wafer bonding

- ***Advanced Packaging***

- 3D Thru Silicon Vias
- Direct Wafer Bonding
- Interposer Technology

- ***Other***

- Embedded waveguides
- Integrated optical elements
- New memory materials
- Photoresist and other polymers
- Magnetic materials (active or shielding)
- Advanced packaging
- 3D IC's and similar device technologies

Segment III Key Points



- Many products not even based on traditional CMOS
- Often adapting silicon CMOS process techniques
- Startup or new entry mentality
- Frequently start on smaller wafer sizes and transition up as volume production increases
- Process flow is generally not mature due to some fraction of “creative” steps
- Design focus = new devices
- Process focus = achieving acceptable yield and ramp

Common Themes



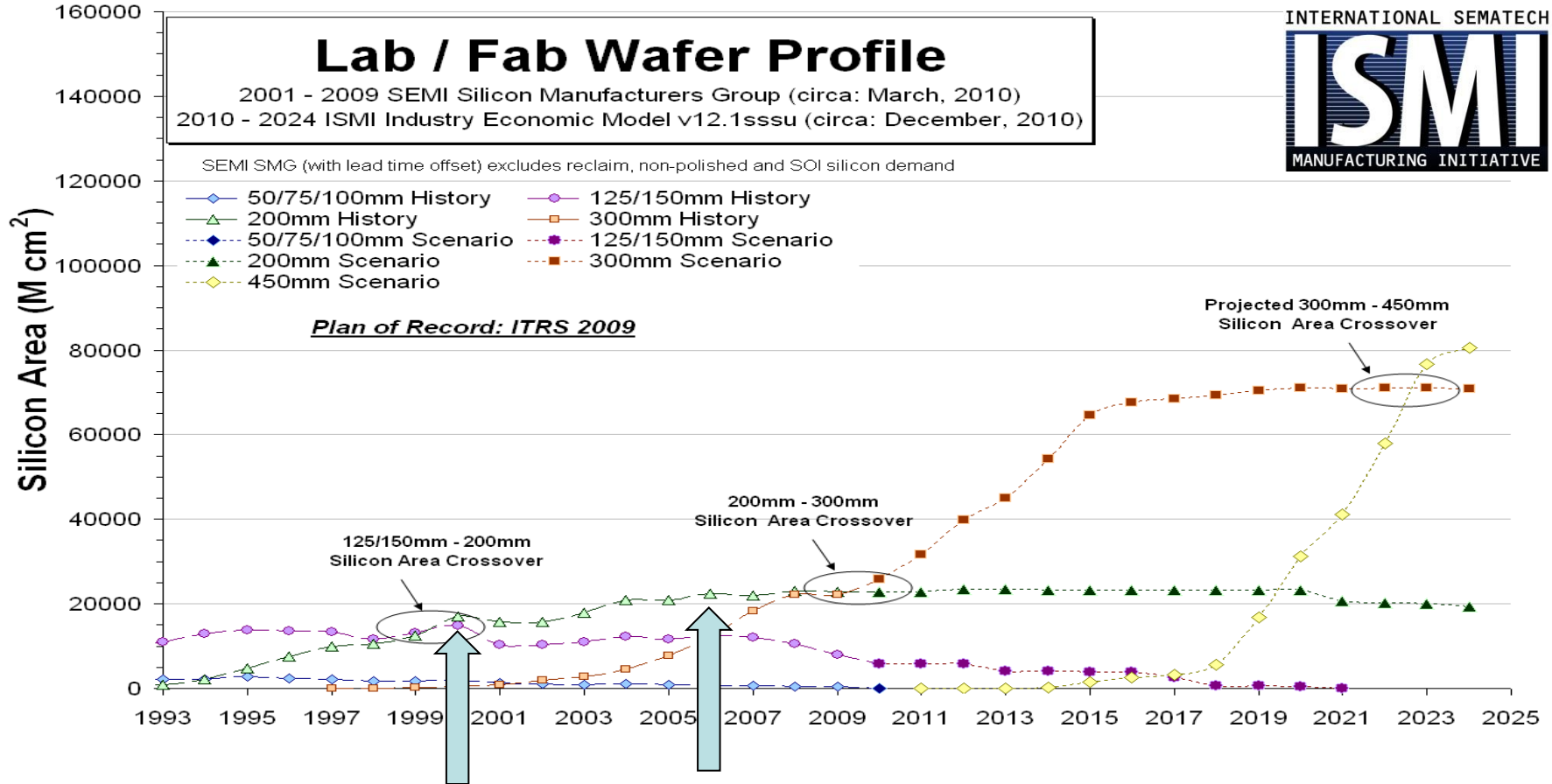
Two common themes have emerged

EXTEND

and

EXPAND

Fab Longevity

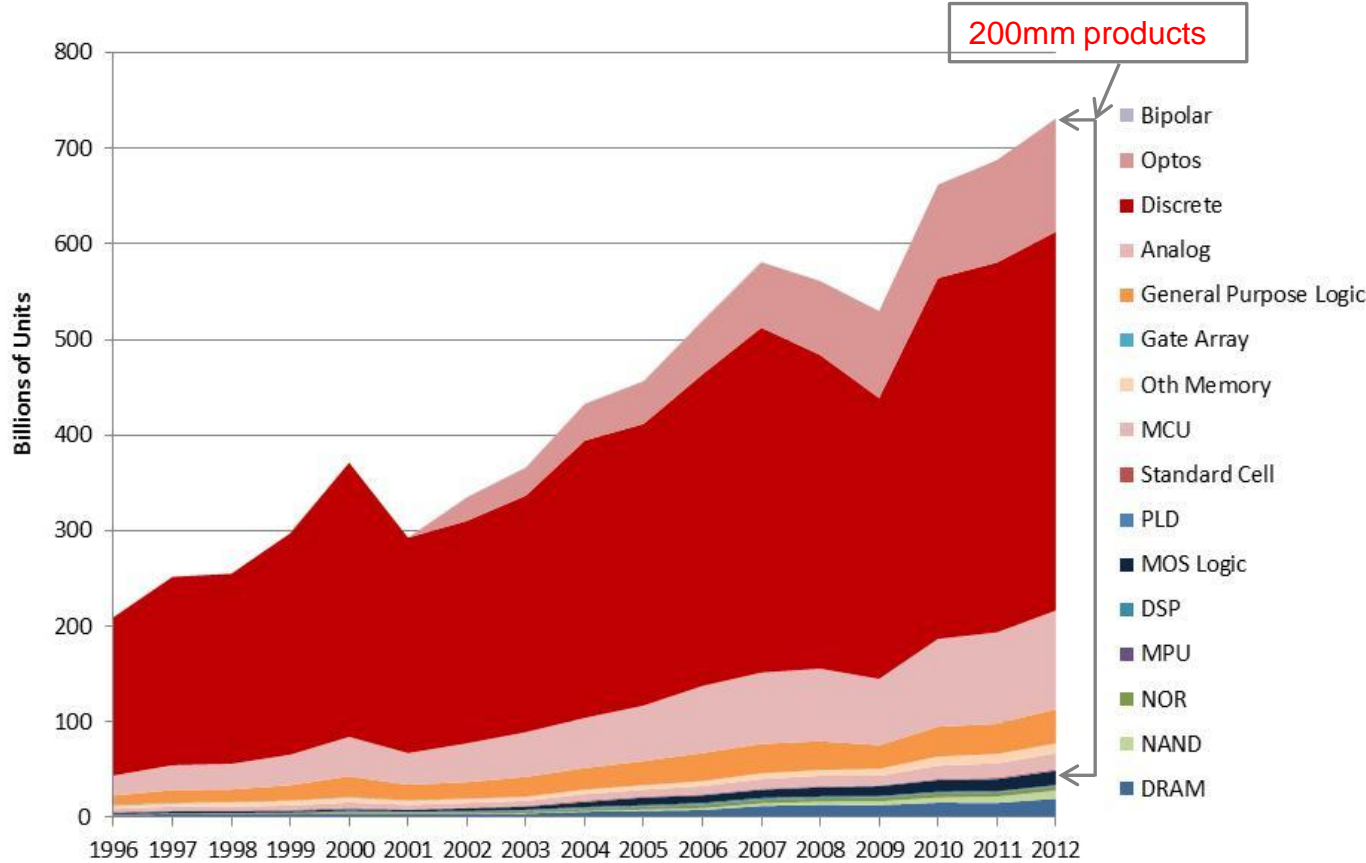


150mm was introduced around 1985, it peaked in 1992. It peaked in 2005 and has steadily decreased since.
 200mm was introduced in 1992. It peaked in 1999 and has steadily decreased since.
 300mm was introduced in 2005, it peaked in 2009 and has remained relatively stable...through 2025!

Fabs & Products Utilizing $\leq 200\text{mm}$ Wafers

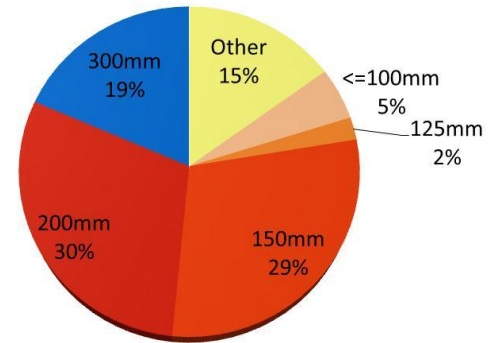


Semiconductor Units from $\leq 200\text{mm}$ Wafers



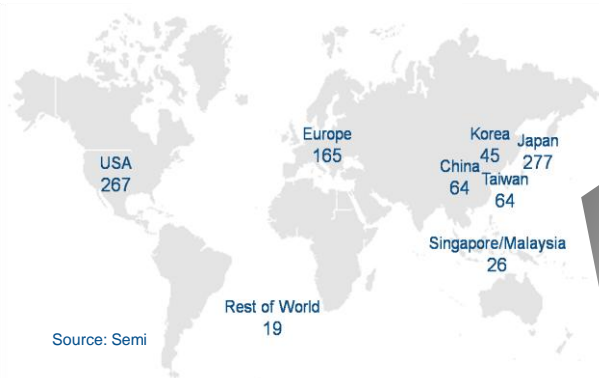
Source: SIA/WSTS and Semico Research Corp

Fabs by Wafer Size



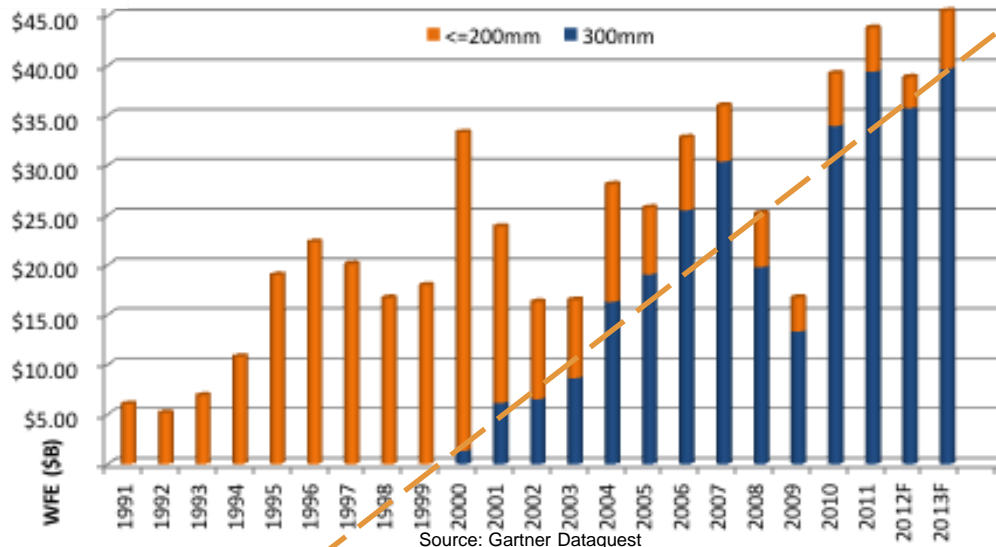
Source: Semico Fab Database

WFE: A Market Divided



>80% of Production Fabs are $\leq 200\text{mm}$
(represents approximately 6M wafers/month)

The Tale and Tail of WFE



Mainstream = More than Moore

- Extend valuable assets
- ROIC

Long-term support:

- Who?
- How?
- What?
- Where?

Leading Edge = More Moore

- Equipment support
- Process support

Long-term support:

- OEM resources



How is any of this information useful?

Management decisions are influenced by certain perspectives and trends. These vary depending on business model and market segment.

| More Moore | |
|----------------------|---|
| DEVICE DESIGN | Push for maximum performance (speed, low power, etc.) Extreme innovation is often necessary |
| EQUIPMENT | Willing to build new fabs or retool existing fabs (extend infrastructure) Drive improvements in both capability and productivity |
| CONSUMABLES | Push performance in nearly every aspect of CMP Defectivity is a primary focus at every CMP process step |
| MATERIALS | Adapt existing materials whenever feasible, but ... Will not hesitate to integrate new materials when necessary |

Decisions



New Mainstream

| | |
|----------------------|--|
| DEVICE DESIGN | Expand product portfolio by leveraging existing process technology More focus on functionality and cost than raw speed |
| EQUIPMENT | Preserve capital and extend life of depreciated tools Buy tools only for "must have" capacity expansions Generally staying on wafer sizes 200mm and below |
| CONSUMABLES | Extreme focus on reducing cost per wafer Defectivity and other factors to improve yield are key |
| MATERIALS | Adapt proven materials and process methods ... period. Optimize process flows for simplicity and yield |

Decisions



Emerging Technology

| | |
|----------------------|---|
| DEVICE DESIGN | Highly customized to the type of device (usually non-CMOS) Startup mentality "find something that works" |
| EQUIPMENT | Preserve capital and minimize overhead Outsourcing is a strong trend (fabless) Generally start at small wafer sizes and work up as volume ramps |
| CONSUMABLES | Not locked in to "traditional" CMP pad/slurry offerings Lots of niche opportunities that are growing as markets evolve |
| MATERIALS | Willing to explore a wide range of materials for unique properties Process requirements vary by several orders of magnitude |

The Future



- Trends vary by segment within the industry
 - More Moore: Continue investment to achieve performance
 - More than Moore: New Mainstream
 - Focus on expanding product portfolio and efficient ROIC
 - More than Moore: Emerging Technologies
 - Focus on new devices or applications (startup mentality)
- Extend the life of existing capital assets
 - Depreciated fabs can be highly profitable
 - Different mindset than previous migration through technology nodes
- Expand range of products made in each fab
 - New designs that utilize existing process technologies
 - Combination technologies (analog/RF, digital/MEMS, etc.)
 - One successful strategy can be to repurpose existing fabs

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