Developing CMP for New Materials and New Integration Schemes

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Overview

Background

CMP Development Cycle

Early Stage Development Examples

Production Qualified Examples

Conclusions and Future Outlook
• Why is development so important? SPEED!
  Faster Development → Faster Chips → Faster Time to Revenue

• Moore’s Law dominates the CMOS industry
  – Not affected by cycles, markets, analysts, or the economy

• Photolithography and CMP are two of the critical process technologies required by manufacturers to continue both cost and performance improvements
  – Photolithography enables SHRINKS
  – CMP enables more complex STACKS

Trend line has held for >35 years !!
Background: CMP Drivers

(1) % of Wafers Using CMP is Increasing

(2) # CMP Polishes per Wafer is Increasing

(3) # CMP Polish Applications is Increasing

(4) Each Application Requires a New CMP Process
CMP Complexity

- **Wafer / Materials Parameters**
  - Size / Shape / Flatness
  - Film Stack Composition
    - Metals (Al, Cu, W, Pt, etc.)
    - Oxide (TEOS, PSG, BPSG, etc.)
    - Other (polysilicon, low-k polymers, etc.)
  - Film Quality Issues
    - Stress (compressive or tensile)
    - Inclusions and other defects
    - Doping or contaminant levels
  - Final Surface Requirements
    - Ultralow surface roughness
    - Extreme planarization, esp. Copper
    - Low defectivity at <0.12 um defect size

- **Pad Issues**
  - Materials (polyurethane, felt, foam, etc.)
  - Properties must be chosen for the job
  - Conditioning method often not optimized
  - Lot-to-lot consistency

- **Slurry Issues**
  - Chemistry optimization often required
  - Mixing and associated inconsistency
  - Shelf life and pot life sometimes very short
  - Slurry distribution system (design, cost, upkeep)
    - Agglomeration and gel formation
    - Filtration is often required
  - Cleaning method specific to slurry and film
  - Waste disposal and local regulations

- **Process Issues**
  - Long list of significant input variables
    - Downforce
    - Platen speed
    - Carrier speed
    - Slurry flow
    - Conditioning method
      - Disk used (material, diamond size, spacing, etc)
      - Force
      - Speed
      - Sweep profile
  - Highly sensitive to local pattern variation
  - Must maintain consistency at high throughput
  - Must optimize for variation of incoming films

- **Integration Issues**
  - Materials Compatibility
    - Electrochemical interactions with two or more metals
    - Film integrity and delamination, esp. low-k
    - Film stack compressibility
  - Interactions with adjacent process modules
    - Photolithography
    - Metal deposition and metal etch
    - Dielectric deposition and etch
  - Electrical design interactions
    - Feature size constraints
    - Interactions with local pattern density
    - Line resistance variation, esp. damascene copper
    - Dielectric thickness variation
    - Contact resistance variation

Any one of these areas can create major headaches for process engineers & integration teams.
CMP is still growing for CMOS applications ... And many newer applications are now also being developed beyond “traditional” CMP.

- **Traditional CMOS Applications**
  - Oxide (ILD, pre-metal dielectric, etc.)
  - Tungsten (plugs or local interconnect)
  - Shallow trench isolation (STI)
  - Polysilicon
  - Copper (integrated with or w/o low-k dielectric)

- **New Apps for CMOS devices**
  - Polymers (both low-k and other uses)
  - Capping layers
  - High-k dielectrics
  - Gate insulators
  - Metal gates
  - Noble metal contacts

- **MEMS**
  - Oxides (doped or undoped)
  - Polysilicon (usually structural)
  - Nitrides and oxynitrides
  - Separation layer (MEMS-first or MEMS-last)

- **Other**
  - Strained layer epi substrates
  - Custom III-IV and II-IV epi layers
  - Phase change memory materials
  - Photoresist and other polymers
  - Magnetic materials (active or shielding)
  - Grating structures
  - Integrated optical layers
  - Advanced packaging
  - 3D IC’s and similar structures
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Conclusions and Future Outlook
Vast majority of development efforts for virtually any process follow this path

Each stage has certain inputs required, activities to be performed, and desired outputs that generally increase in difficulty and complexity as the project moves forward.

Each stage assumes successful completion of the previous stage, or at least overlapping execution of the previous stage.

Failure at any stage generally means moving back at least one stage to try again.
**First series of stages … Design Concept through Prototype**

<table>
<thead>
<tr>
<th>Stage</th>
<th>Resources</th>
<th>Activities</th>
<th>Stage Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Design Concept</strong></td>
<td>Designers</td>
<td>1. Brainstorming</td>
<td>Approval from R&amp;D team, management for design approach &amp; use of CMP</td>
</tr>
<tr>
<td></td>
<td>R&amp;D team</td>
<td>2. Sketches/drawings/etc.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Documentation</td>
<td></td>
</tr>
<tr>
<td><strong>Materials Selection</strong></td>
<td>Designers</td>
<td>1. Assess extendability of existing materials &amp; processes</td>
<td>List of primary materials and backups, if possible, for all materials to be polished</td>
</tr>
<tr>
<td></td>
<td>R&amp;D team</td>
<td>2. Propose/evaluate alternatives</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Materials scientists</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Integration Planning</strong></td>
<td>Designers</td>
<td>1. Assess extendability of integration &amp; process flow</td>
<td>First pass process flow showing each CMP level</td>
</tr>
<tr>
<td></td>
<td>R&amp;D team</td>
<td>2. Propose alternatives</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Integration team</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Process Development</strong></td>
<td>Integration team</td>
<td>1. Process screening expt</td>
<td>Demonstration of initial process for new materials, new modules or processes needing major improvements</td>
</tr>
<tr>
<td></td>
<td>Process engineering</td>
<td>2. Repeat trials until acceptable performance on blanket films</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Test wafers</td>
<td>3. Early pattern test wafers (maybe)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Eng time on process tools</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Device Prototype</strong></td>
<td>Integration team</td>
<td>1. First silicon on new masks</td>
<td>One or a few working devices &amp; proposals for improving any critical path items</td>
</tr>
<tr>
<td></td>
<td>Process engineering</td>
<td>2. Lots of analysis (SEM, etc.)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Analytical support team</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Wafers &amp; process tool (eng)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Generic CMP Integration (2)

Stages leading to revenue … Optimization through HVM

<table>
<thead>
<tr>
<th>Stage</th>
<th>Resources</th>
<th>Activities</th>
<th>Stage Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optimization</td>
<td>Integration team</td>
<td>1. Refine CMP process based on details from first silicon</td>
<td>Iterative improvements until acceptable performance and yield are achieved</td>
</tr>
<tr>
<td></td>
<td>Process engineering</td>
<td>2. Explore process windows</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Analytical support team</td>
<td>3. Repeat trials (consistency)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Wafers &amp; process tools (1x)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Qualification</td>
<td>Engineering teams</td>
<td>1. Produce live devices for qual</td>
<td>Devices for burn-in &amp; life test</td>
</tr>
<tr>
<td></td>
<td>Manufacturing teams</td>
<td>2. Prep for transfer to mfg</td>
<td>Documentation in place for each process step</td>
</tr>
<tr>
<td></td>
<td>Wafers &amp; process tools (1x)</td>
<td>3. Establish initial SPC limits</td>
<td></td>
</tr>
<tr>
<td>Pilot Production</td>
<td>Manufacturing teams</td>
<td>1. Transfer control to mfg</td>
<td>Sellable devices</td>
</tr>
<tr>
<td></td>
<td>Engineering teams</td>
<td>2. Monitor device and process metrics for signs of instability</td>
<td>Assessment of any issues showing up as volume ramps</td>
</tr>
<tr>
<td></td>
<td>Wafers</td>
<td>3. Refine and lock SPC limits</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Process tools (multiple)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Volume Manufacturing</td>
<td>Manufacturing teams</td>
<td>1. Manufacturing controls</td>
<td>Profitable devices</td>
</tr>
<tr>
<td></td>
<td>Engineering teams</td>
<td>2. Monitor SPC trends</td>
<td>Technical inputs for next gen device designs</td>
</tr>
<tr>
<td></td>
<td>Wafers</td>
<td>3. ID yield/cost improvement targets &amp; requal when justified</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Process tools (multiple)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CMP Process Development and Optimization

- Zoom in on CMP process development and optimization phases
- Test wafer availability and quality often impacts timeline, validity of results, etc.
- Initial process DOE’s generally focus on removal rate and gross surface quality
- Optimization stages can be interchanged or executed in parallel
- Planarity can mean step height, dishing, erosion, roughness, etc. depending on the material and intended application
- Failure at any stage generally means moving back at least one stage to try again
CMP processes are generally measured on these parameters:

- **Removal Rate and Uniformity**
- **Defectivity**
- **Planarization Capability**
  (step height, dishing/erosion, surface roughness, etc.)
- **Process Stability**
  (repeatability for wfr-to-wfr, run-to-run, etc.)
- **Cost per Wafer**
Overview

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CMP Development Cycle

Early Stage Development Examples

Production Qualified Examples

Conclusions and Future Outlook
Early stage development efforts often involve:

- Immature deposition or growth processes
- Poorly characterized materials or integrations
- Technologists who may not be familiar with CMP and how it interacts with other processes
- Wide variation in pattern density/feature sizes
- Wafer sizes smaller than 200mm
- Limited availability of test wafers

**These factors create huge challenges at CMP**
### Example: SiGe Epi

**Process Factors:**
- Standard Si process left Ra too high
- Post-CMP clean had to be developed
- Composition varied widely

<table>
<thead>
<tr>
<th>Metric</th>
<th>Incoming Value</th>
<th>Target</th>
<th>Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Surface Roughness, Ra</td>
<td>&gt;10 nm</td>
<td>&lt;1 nm</td>
<td>0.2-1.4 nm</td>
</tr>
<tr>
<td>Removal Rate</td>
<td>n/a</td>
<td>&gt;500 A/min</td>
<td>480-1600 A/min</td>
</tr>
<tr>
<td>Total Mtrl Removal</td>
<td>n/a</td>
<td>0.25-0.75 um</td>
<td>Within 5%</td>
</tr>
</tbody>
</table>

![Graph showing Epi Layer %Ge vs Polish Rate (Ang/min)](image)

![Bar chart showing Roughness, Ra (nm) before and after CMP](image)
Example: BPTEOS on Si3N4

<table>
<thead>
<tr>
<th>Example Parameter</th>
<th>Value or Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top layer material</td>
<td>BPTEOS oxide</td>
</tr>
<tr>
<td>Bottom layer material</td>
<td>LPCVD silicon nitride</td>
</tr>
<tr>
<td>BPTEOS removal rate</td>
<td>4900 Ang/min</td>
</tr>
<tr>
<td>Selectivity (BPTEOS:SiN)</td>
<td>&gt;25 : 1</td>
</tr>
<tr>
<td>Planarization Efficiency</td>
<td>&gt; 98%</td>
</tr>
</tbody>
</table>

**Example:**

**BPTEOS on Silicon Nitride**

- Topography was coated with uniform layer of BPTEOS
- Stopping layer was relatively thin
- Goal of CMP process is to stop on nitride without breaking through and planarize across all inlaid features

**Process Factors**

- Multiple pads & slurries were screened
- Overpolish margin had to be > 30%
- Similar to shallow trench process
Example: Poly on Oxide

- Pattern cut into Si wafer
- Deposit thin oxide layer then grow polysilicon onto entire surface
- Goal of CMP process is to stop on thin oxide without breaking through and planarize across all inlaid features
- Multiple pads and slurries screened
- Demonstrated materials integration concept for future design inputs

<table>
<thead>
<tr>
<th>Example Parameter</th>
<th>Value or Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top layer material</td>
<td>Polysilicon</td>
</tr>
<tr>
<td>Bottom layer material</td>
<td>Oxide (undoped)</td>
</tr>
<tr>
<td>PolySi removal rate</td>
<td>4100 Ang/min</td>
</tr>
<tr>
<td>Selectivity (PolySi:Oxide)</td>
<td>&gt;100 : 1</td>
</tr>
<tr>
<td>Planarization Efficiency</td>
<td>&gt; 99%</td>
</tr>
</tbody>
</table>

Polysilicon plug

Thin oxide layer (capping oxide added for SEM prep)
Early Stage Development

In general, the key requirements for early stages of CMP development are:

• Strong understanding of materials and key integration issues likely to occur with CMP
• Fully capable process equipment and metrology
• Depth of CMP process expertise
• Creativity and innovation

Successful early stage efforts lead to working prototype devices and sufficient understanding to move forward with qual...
Overview

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Early Stage Development Examples

Production Qualification Examples

Conclusions and Future Outlook
• Development team stays heavily involved through qualification
• Handoff to manufacturing team generally occurs during pilot production
• Requirements for smooth transition include:
  – Documented procedures
  – SPC (at least initial limits)
  – Training of manufacturing staff (operators, techs, sustaining eng, etc.)
  – Followup of any issues uncovered during initial ramp
• Same basic requirements apply to qualifying an outsource facility

Next Example: Qualifying an oxide CMP process
Blanket Wafer Marathon

Process stability across 250-wafer extended run combining fillers & rate wafers

Oxide CMP Qualification Run
Polisher: AMAT Mirra Mesa
Pad: IC1010
Slurry: Klebosol 1501-50
Conditioning: In-situ
Metrology: 49-point diameter scan, 3mm EE
Defectivity across 250-wafer extended run

Mesa Cleaner: 2% NH₄OH in both brush stations
Metrology Platform: AMAT Orbot
Remaining Qual Metrics

- Post-CMP residual surface contamination (shown in table at left) was compared between existing qualified process and desired outsource process – no differences were observed

- Planarization efficiency was compared on test wafers (data not shown) to verify that results were exactly equivalent

- Based on accumulated data, authorization was obtained to run product split lots to compare device yield

<table>
<thead>
<tr>
<th>Element</th>
<th>Fab Reference</th>
<th>Entrepix Polisher #1</th>
<th>Entrepix Polisher #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>354.86</td>
<td>440.95</td>
<td>268.84</td>
</tr>
<tr>
<td>Cl</td>
<td>33.8</td>
<td>62.63</td>
<td>65.46</td>
</tr>
<tr>
<td>K</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Ca</td>
<td>2.35</td>
<td>2.89</td>
<td>3.21</td>
</tr>
<tr>
<td>Sc</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Ti</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>V</td>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Cr</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Mn</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>Fe</td>
<td>0</td>
<td>0</td>
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<tr>
<td>Co</td>
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<tr>
<td>Ni</td>
<td>0</td>
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<td>Cu</td>
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<tr>
<td>Zn</td>
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<tr>
<td>W</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

All Units = 1E10 atoms/cm²
Split Lot Yield

Product yield equivalent between all split lot groups

→ Qualification complete for outsource production
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Conclusions and Future Outlook
• Rapid development of new device technology is required for a fab to remain competitive
• Shrinking design rules and stacking of additional layers continue to drive more volume and more complexity for CMP in CMOS flows
• Many new device technologies also require CMP
• New materials or new integrations usually require new CMP processes
  – Some may be reoptimized extensions of an existing CMP process
  – Others may require development of completely new pads or slurries
• CMP process development generally proceeds along a consistent sequence of stages
• Each generation of device technology drives another cycle of increased demands on CMP process technology
Anyone desiring copies of this presentation or any other information can contact any of the following individuals:

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