Developing Products for CMP Requires a Module-Level Approach

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Presented at CAMP Conference – August 2007
Outline

• CMP complexity – the process puzzle

• Module level integration issues with different chemistries
  • Case study 1: insufficient inhibitor
  • Case study 2: excess inhibitor

• Summary and Conclusions
New Applications

CMP is still evolving for CMOS applications ... And many newer applications are now also being developed beyond “traditional” CMP.

**MEMS**
- Oxides (doped or undoped)
- Polysilicon (usually structural)
- Nitrides and oxynitrides
- Separation layer (MEMS-first or MEMS-last)
- Metals (esp. for reflective surfaces)

**Integrated Optics**
- Grating structures
- Embedded waveguides
- Integrated optical elements

**Advanced Substrates**
- Strained layer epi substrates
- Custom III-IV and II-IV epi layers
- SOI
- GaN, GaP, SiC, etc.
- Various surfaces for direct wafer bonding

**Other**
- Phase change memory materials
- Photoresist and other polymers
- Magnetic materials (active or shielding)
- Advanced packaging
- 3D IC’s and similar device technologies
CMP Process Puzzle

CMP JIGSAW PUZZLE

- Material
- Platen Speed
- Slurries
- Process
- Conditioning
- Backing Films
- Downforce
- Pads
- Carrier Speed
- Slurry Flow
- Pattern Density
- Swep Profile
- Film Stacks
- Compressibility
- Integration
- Film Quality
- Consumables Variation
- Compatibility
- Cleaning Chemistry
- Scratching
- Dishing
- Delamination
- Waste Disposal
- Slurry Distribution
- Defectivity
- Erosion
- Planarity

CMP FastForward™

entrepix YOUR CMP PARTNER

ATMI and Entrepix confidential
CMP Complexity

Wafer / Materials Parameters
- Size / Shape / Flatness
- Film Stack Composition
  - Metals (Al, Cu, W, Pt, etc.)
  - Oxide (TEOS, PSG, BPSG, etc.)
  - Other (polysilicon, low-k polymers, etc.)
- Film Quality Issues
  - Stress (compressive or tensile)
  - Inclusions and other defects
  - Doping or contaminant levels
- Final Surface Requirements
  - Ultralow surface roughness
  - Extreme planarization, esp. Copper
  - Low defectivity at <0.12 um defect size

Process Issues
- Long list of significant input variables
  - Downforce
  - Platen speed
  - Carrier speed
  - Slurry flow
  - Conditioning method
    - Disk used (material, diamond size, spacing, etc)
    - Force
    - Speed
    - Sweep profile
- Highly sensitive to local pattern variation
- Must maintain consistency at high throughput
- Must optimize for variation of incoming films

Integration Issues
- Materials Compatibility
  - Electrochemical interactions with two or more metals
  - Film integrity and delamination, esp. low-k
  - Film stack compressibility
- Interactions with adjacent process modules
  - Photolithography
  - Metal deposition and metal etch
  - Dielectric deposition and etch
- Electrical design interactions
  - Feature size constraints
  - Interactions with local pattern density
  - Line resistance variation, esp. damascene copper
  - Dielectric thickness variation
  - Contact resistance variation

Pad Issues
- Materials (polyurethane, felt, foam, etc.)
- Properties must be chosen for the job
- Conditioning method often not optimized
- Lot-to-lot consistency

Slurry Issues
- Chemistry optimization often required
- Mixing and associated inconsistency
- Shelf life and pot life sometimes very short
- Slurry distribution system (design, cost, upkeep)
  - Agglomeration and gel formation
  - Filtration is often required
- Cleaning method specific to slurry and film
- Waste disposal and local regulations

Process development teams must balance complexity, cost, risk, and timelines.
Generic CMP Process Sequence

**INPUTS**
- Pad
- Slurry
- Process Settings
- Film Properties
- Etc.

**METRICS**
- Cu Rate
- Cu Uniformity
- Planarization
- Cu Rate
- Cu Uniformity
- Ta Rate
- Ta Uniformity
- Dishing
- Erosion
- Cu Surface
- Cu Rate
- Cu Uniformity
- Ta Rate
- Ta Uniformity
- Dielectric Rate
- Dielectric Unif.
- Dishing
- Erosion
- Roughness (all mtrls)
- Etc.

Linearized representation of AMAT Relexion or Mirra Mesa or similar CMP process equipment
Case Study 1: Insufficient Inhibitor Coverage

**INPUTS**

- ATMI
  - Cu Slurry A: Inhibitor A
  - Rinse: None
- Competitor
  - Barrier Slurry B: Inhibitor B

**METRICS**

- Wafer
- P1
- P2
- P3
- CLEANING MODULE
- Wafer

- Cu Surface: Coverage with inhibitor A
- Corrosion
Corrosion Pits Observed at Customer Trial: Cu Slurry A Used with Barrier Slurry B

- Observation of small corrosion pits
- Defect density was at saturation level of the metrology tool
- Baseline process, i.e. POR Cu slurry and barrier slurry B, did not display high defect count
Where Did We Go Wrong?
Retracing steps

Root cause analysis:
Attempt to recreate customer trial results by looking at corrosion protection during
• Cu polish
• Post Cu polish rinse procedure
• Barrier polish
Post Cu Polish: Wafer Maps of Tool Fault and Control Wafers

No corrosion evident after 15 minute tool fault (same results for 30 min, data not shown)
Total defect counts were 35 for tool fault and 41 for control
Post P2 Rinse Procedure Evaluation:
No Observation of Pitting During ATMI In-House Trial

4 Different experimental conditions:

- Slurry A
- HPR
- Inhibitor B rinse
- Pad clean

Conditions during customer trial
- Slurry A
- HPR
- Pad clean
- (same result using inhibitor B rinse at end)

No pitting observed on ATMI wafers (same node as customer test wafer)
- Based on overall defect levels, inhibitor B rinse does not affect defectivity levels.

=> Pitting does not occur during or right after P2 polish
Post P2 Rinse Procedure Evaluation:
No Observation of Pitting During ATMI In-House Trial

Summary of experimental results in the process flow diagram:

INPUTS
Using wafers with same node as customer's

ATMI
Cu Slurry A:
Inhibitor A
Rinse:
Various iterations

Anji
Barrier Slurries:
A (acidic)
Inhibitor B&C

METRICS
Cu Surface:
Coverage with inhibitor A and/or B
No corrosion

CLEANING MODULE
No corrosion

Wafer
P1
P2
P3
Wafer
Verifying Customer Plating Chemistry

During additional in-house evaluations, MIT854 wafers were plated using customer’s plating chemistry and process settings (ECD bath parameters), then polished to check for pitting post P2.

The result did not show any pitting observed after copper polish (P2):

- Similar ECD bath did not result in copper pitting
- Pitting was checked using the full-wafer SEM, looking at 180nm L/S arrays.
Table Top Experiment – Barrier Slurry A

Process Sequence
• Cu slurry A
• HPR
• Pad clean
• Barrier slurry A

Objective of this experiment was to verify compatibility with a silica based, acidic barrier slurry (ATMI/Anji in-house trial) using wafers plated with customer’s ECD process.

Slurry residuals due to coupon work
• Wafer was not cleaned post CMP

Results
• No pitting observed on the wafer
Table Top Experiment – Barrier Slurry D

Process Sequence
- Cu slurry A
- HPR
- Pad clean
- Barrier slurry D

Objective of this experiment was to verify compatibility with a silica based, alkaline barrier slurry (ATMI/Anji in-house trial) using wafers plated with customer’s ECD process

Slurry residuals due to coupon work
- Wafer was not cleaned post CMP

Results
- No pitting observed on the wafer
Attempt to Reproduce Corrosion Defects: Looking for Pitting Corrosion Post P3

**INPUTS**
- Using customer's plating process

**ATMI**
- Cu Slurry A: A (acidic)
- Inhibitor A
- Rinse: D (alkaline)
- No inhibitor B

**Anji**
- Barrier slurries: A (acidic)
- Inhibitor B&C
- D (alkaline)
- Inhibitor D

**METRICS**
- Cu Surface: No corrosion
- Coverage with inhibitor A
- No corrosion
- No corrosion

**CLEANING MODULE**
Problem Resolution: Change Rinse Process

**INPUTS**
- ATMI
  - Cu Slurry A: Inhibitor A
  - Rinse: Inhibitor B
- Competitor
  - Barrier Slurry B: Inhibitor B

**METRICS**
- Cu Surface: Coverage with inhibitor B
- No corrosion

**Diagram**

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[Diagram showing the process flow from Wafer to Wafer through P1, P2, P3, and the Cleaning Module]
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Summary

• Corrosion occurred only for a particular combination of Cu slurry, rinse procedure and barrier slurry
• In order to prevent corrosion during the barrier slurry polish, the Cu surface required sufficient coverage of a particular inhibitor
Case Study 2: Excess Inhibitor Coverage

Anji TCU2000H4
And Clean A

0.136/cm²

Cu Surface: Coverage with inhibitor B&C
Defectivity: No organic residues
Defect Wafer Maps

ATMI Barrier Slurry Veridium 2 contains inhibitor D

ATMI Clean A contains inhibitor D

P3 → CLEANING MODULE → Wafer

Cu Surface: Defectivity Coverage with inhibitor D Organic residues

Veridium 2 Clean A

Defectivity: 2.979/cm², 5.017/cm², 6.107/cm²
Defect Images

Defects are mostly found on Cu features
They appear as dark agglomerates or polymeric residuals
Counts per wafer ~ 1000, random distribution
Problem Resolution: Remove Inhibitor D from Clean A

Summary:
- The difference in Cu surface coverage depending on the inhibitor used in the barrier slurry may lead to incompatibilities with the cleaning chemistry.
- Excess amounts of inhibitor concentrations can form precipitates in the form of organic residues.
Conclusion

• Severe defect issues may arise from the incompatibility of individual CMP process steps, e.g. Cu polish, rinse, barrier polish, clean etc.

• Individual chemicals for the CMP module are only likely to succeed if they perform in concert with the other chemistries utilized
CMP processes are generally measured on these parameters:

- Removal Rate and Uniformity
- Defectivity
- Planarization Capability (step height, dishing/erosion, surface roughness, etc.)
- Process Stability (repeatability for wfr-to-wfr, run-to-run, pad life, etc.)
- Cost per Wafer
30 min tool default wafer

BGSH32435.1-COPPER_CMP-594WSB0
2006-05-16 15:42:35
Product: L354
Process: COPPER_CMP
Lot: BGSH32435.1
Wafer: 594WSB0
Slot: 25
Defects: 86
Density: 0.725
SEM Images: 32
Step 1 Slurry: Cerulean 4 - 041262P
Step 2 Slurry:

0.725/cm²

BMH4235.1-COPPER_CMP-594WSB0

Ti corrosion study wafer. Wafer was dechucked over the platen with high pressure rinse on for 30 min. No Ip12, no rinse post polish to simulate worst possible condition. Head rotating slowly, platen stopped.

FM: 22 0.499
NV: 10 0.227
Generic CMP process development and optimization phases

Test wafer availability and quality often impacts timeline, validity of results, etc.

Initial process DOE’s generally focus on removal rate and gross surface quality

Optimization stages can be interchanged or executed in parallel

Planarity can mean step height, dishing, erosion, roughness, etc. depending on the material and intended application

Failure at any stage generally means moving back at least one stage to try again