Advances in CMP for TSV Reveal

Robert L. Rhoades and Dean Malta
Presentation for ICPT – October 2012
Grenoble, France

entrepix
YOUR CMP PARTNER

Outline

TSV's and the Role of CMP

TSV Reveal (non-selective)

TSV Reveal After Si Etch

Summary

Background

- Two-dimensional device scaling is increasingly difficult and fast approaching fundamental limits of physics (or balance sheets).
- 3D integration also faces substantial process and design issues, but various approaches are now gaining traction.
- Timing for mainstream adoption of 3D is now. Several products are already in the market and more are being launched.
- One of the key technologies to enable 3D structures is TSV’s.

3D Packaging Apps

MCP

Vias : > 20 µm
Holes : < 1000
t = 50 µm

NAND

2 "3D TSV Stack" Era

DRAM

Si Interposer

4 "3D Logic-SiP" Era

Embeded memory

Vias : 5-20 µm
Holes : > 100K
t < 100 µm

Logic

POP

3D SiP

5 Ultimate 3D IC

MEMS
Logic
Analog
RF
DRAM
MPU

Vias < 1 µm
Holes > 100K
t < 20 µm

Vias : > 50 µm
Holes : < 50
t > 200 µm

1 "3D-WLP" Era

RF-SiP

WLP RF-SiP

3D RF-SiP

Passive

MEMS

WLP MEMS

3D CIS

Vias = 10-30 µm
Holes < 100
t < 50 µm

CIS

WL-CSP CIS

TSV CIS

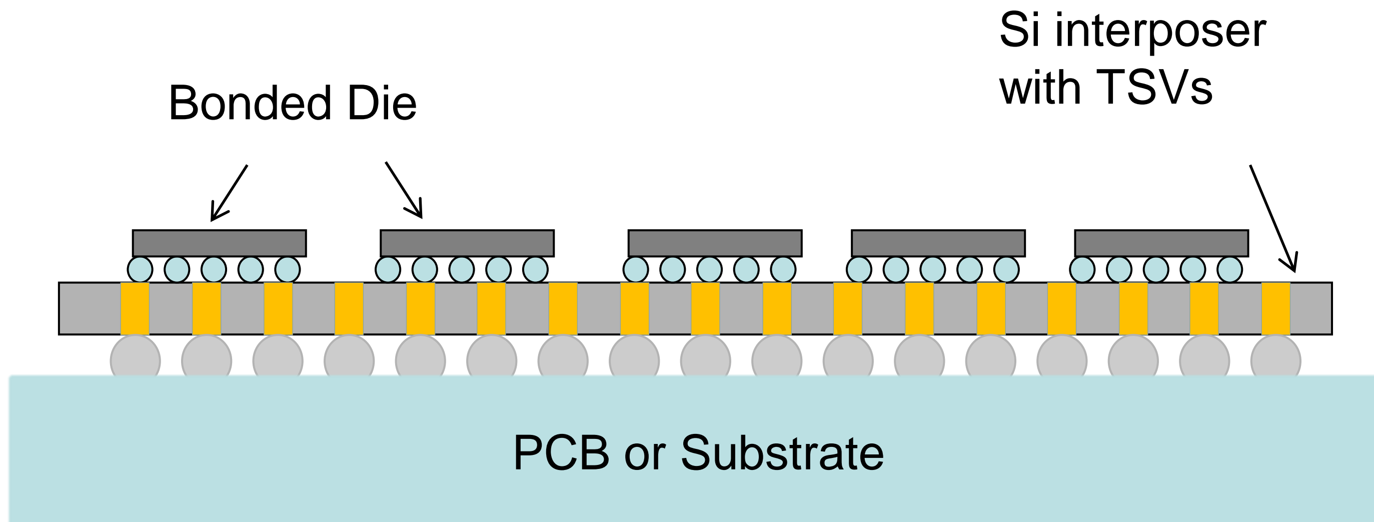
SOC CIS

3 "3D Fusion" Era

Source: Yole Developmentt

2005 2006 2007 2008 2009 2010 2011 2012 2013 2014

2.5D Integration



Source: RTI

Interposers

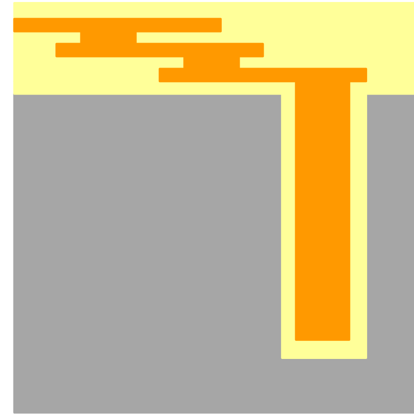
- Viewed as more cost-effective with many current designs
- Allow more flexibility in device architecture and PCB layout
- Stepping stone to full 3D integration

Role of CMP

- CMP is used in a damascene architecture to form the via after the conductor deposition from one side.
- TSV's can be filled with any of several conductive materials.
  - Most common options are copper and polysilicon.
  - Final choice depends on dimensions, operating voltage and current, frequency, plus other integration factors.
- CMP is used again (sometimes multiple steps) after backgrind to help expose and planarize the "bottom" of the TSV's.
- Topography requirements are generally much less demanding than CMOS interconnect levels.

Process Flow

(a)



(b)

(c)

(d)

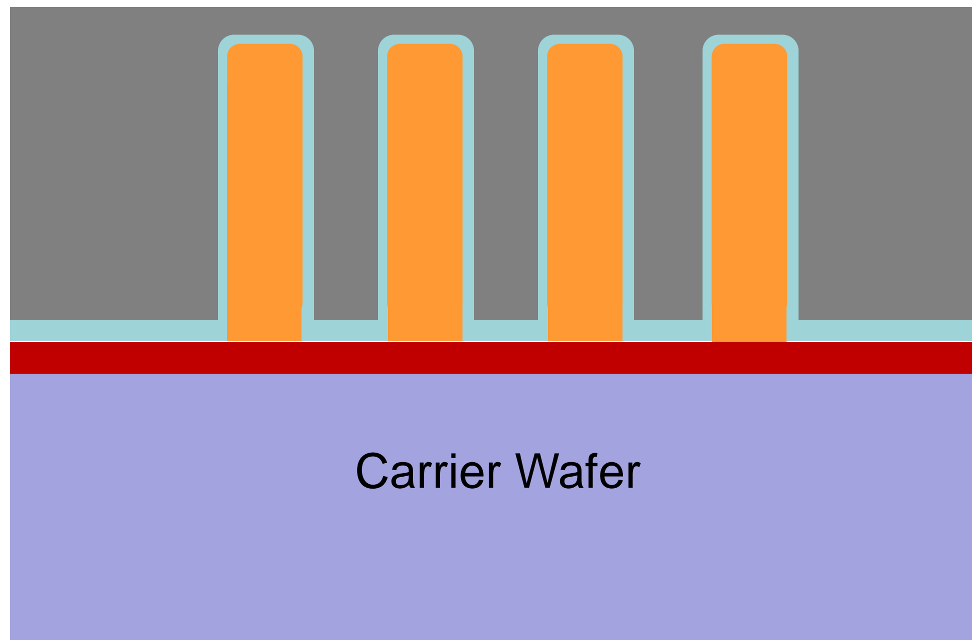
Process flow for Si interposer with TSVs: (a) TSV etch, isolation layer, plating, and via CMP,
(b) Frontside multi-level metallization, (c) Wafer thinning and TSV reveal, (d) Backside metallization.

TSV Reveal

- Process module following completion of device layers on front side
- TSV must be exposed to make contact and/or continue patterning next layers (RDL) from wafer backside.
- Various integrations are being pursued with combinations of backgrind, etch, selective CMP, or non-selective CMP.
  - Some approaches require 2 or 3 steps of CMP to achieve desired result
- Two alternatives with very different requirements for CMP
- Example 1: Reveal Using Non-selective CMP
- Example 2: Reveal CMP Following Si Etch

Non-Selective Reveal

Backgrind stops in Si before reaching TSV's



Carrier Mount

- TSV wafers mounted face down on carrier wafers

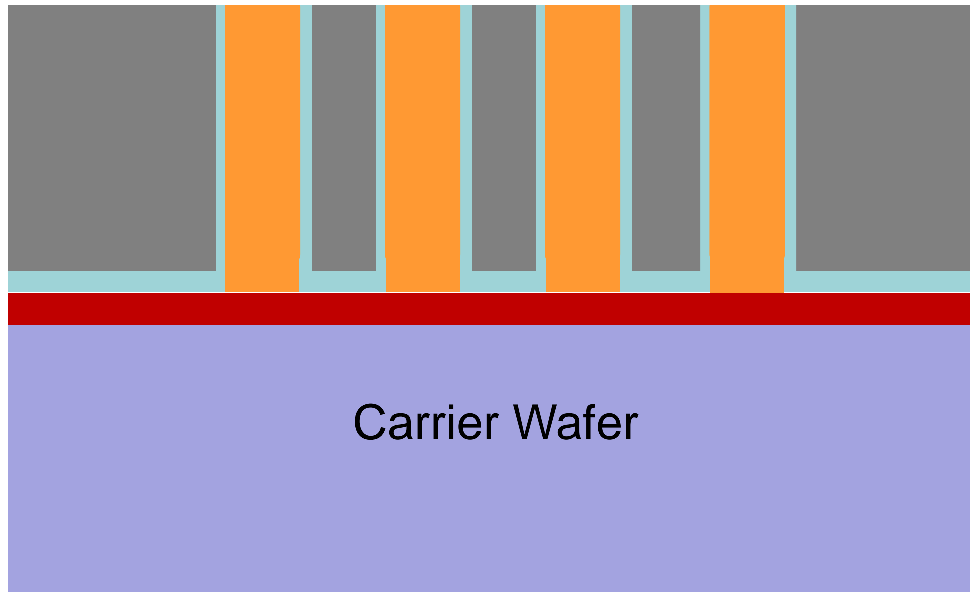
Backgrind

- TSV wafers thinned using backgrind to approx 3-15um "below" TSVs

- Reveal CMP performs dual function of removing grind damage layer and remaining bulk Si then exposing center conductor of TSV's

Reveal CMP #1

Expose & Planarize TSVs

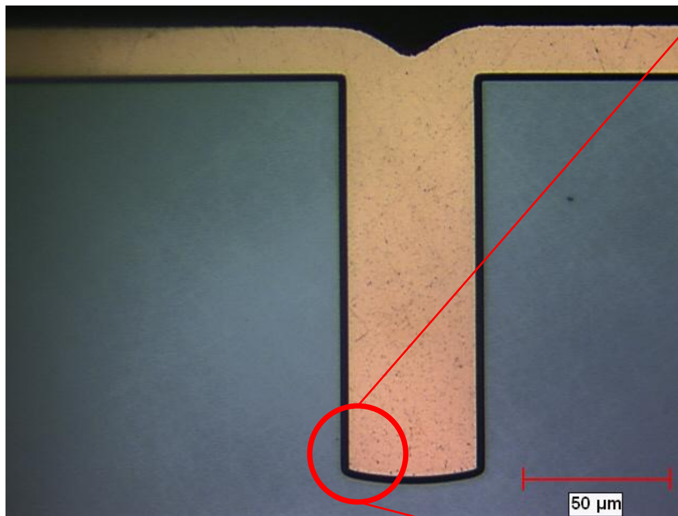


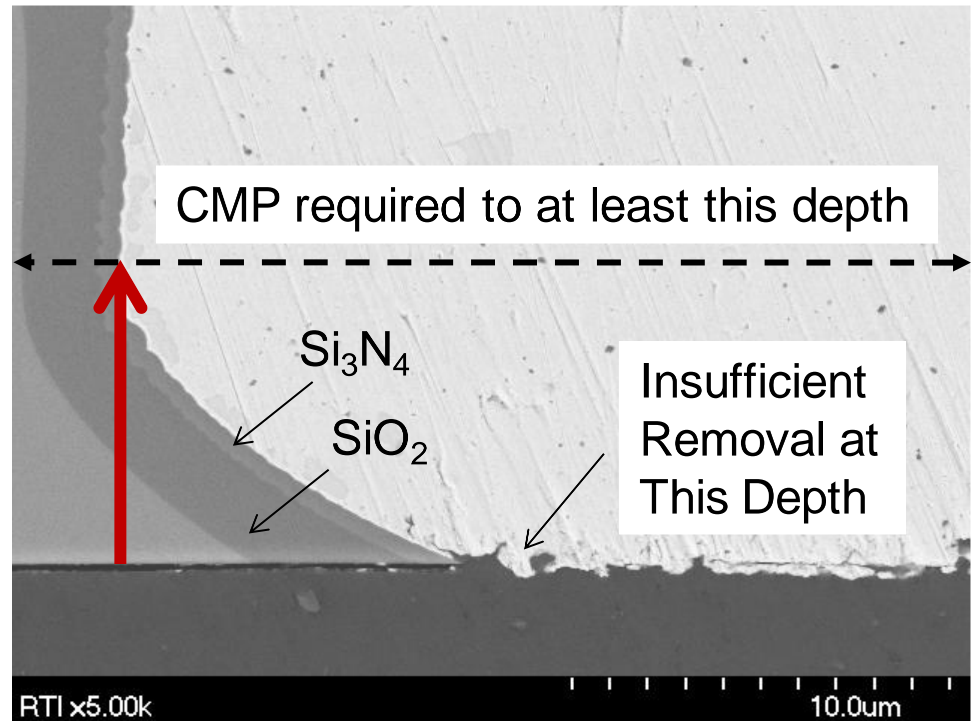
<u>Several exposed materials</u>

- Single crystal silicon
- Oxide (or other liner)
- Barrier metal
- Copper

Architecture

Need to polish far enough into TSVs to remove rounded profile at base of vias





CMP Process Goals

- High Si rate
- Low selectivity
  - Reasonably matched Cu and Tox rates
  - Non-zero barrier metal rate (though usually thin layer)
- Good planarization
  - Low dishing if wide features are present
- Good surface quality
  - Low roughness on both Si and Cu
  - No scratching
  - Not as stringent as CMOS metallization

CMP Slurry Screening

Removal Rate (Ang/min)

10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0

Si Rate
Cu Rate
Oxide Rate

Slurry A
Slurry B
Slurry C
Slurry D
Slurry E
Slurry F
Slurry G
Slurry H
Slurry I
Slurry J

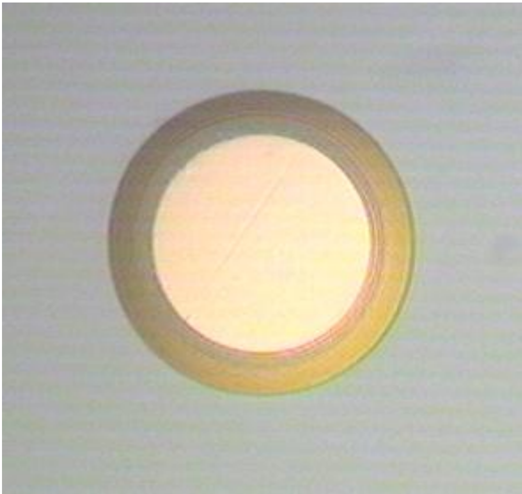
entrepix
Our Expertise,
Our Services,
Your Success

Same process settings used on all screening tests

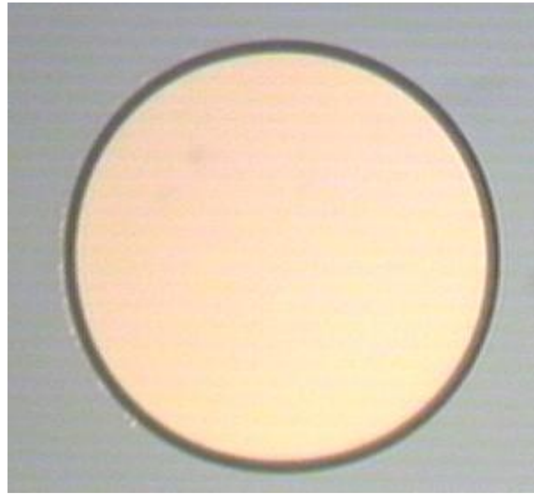
CMP Process

- Slurry J was chosen for patterned wafers
- Re-optimized process for higher Si rate
  - Target 1 um/min → Achieved 1.05 um/min
- Iterative polish on first wafer
  - Total amount to be removed estimated at 30 um
  - Polished in 5 minute increments
  - Inspection clearly showed breakthrough
  - Final surface topography <250 nm achieved

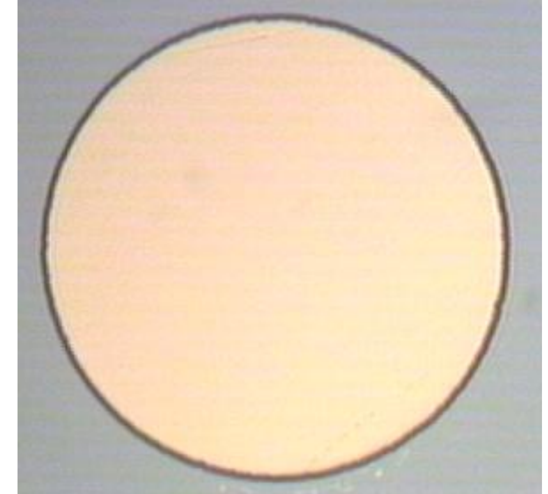
Visual endpoint



20 min



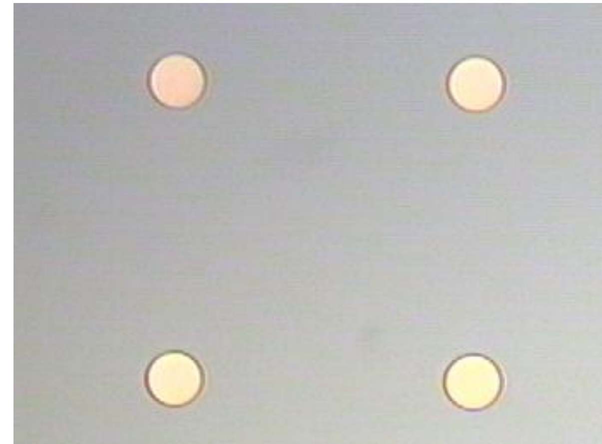
25 min



30 min

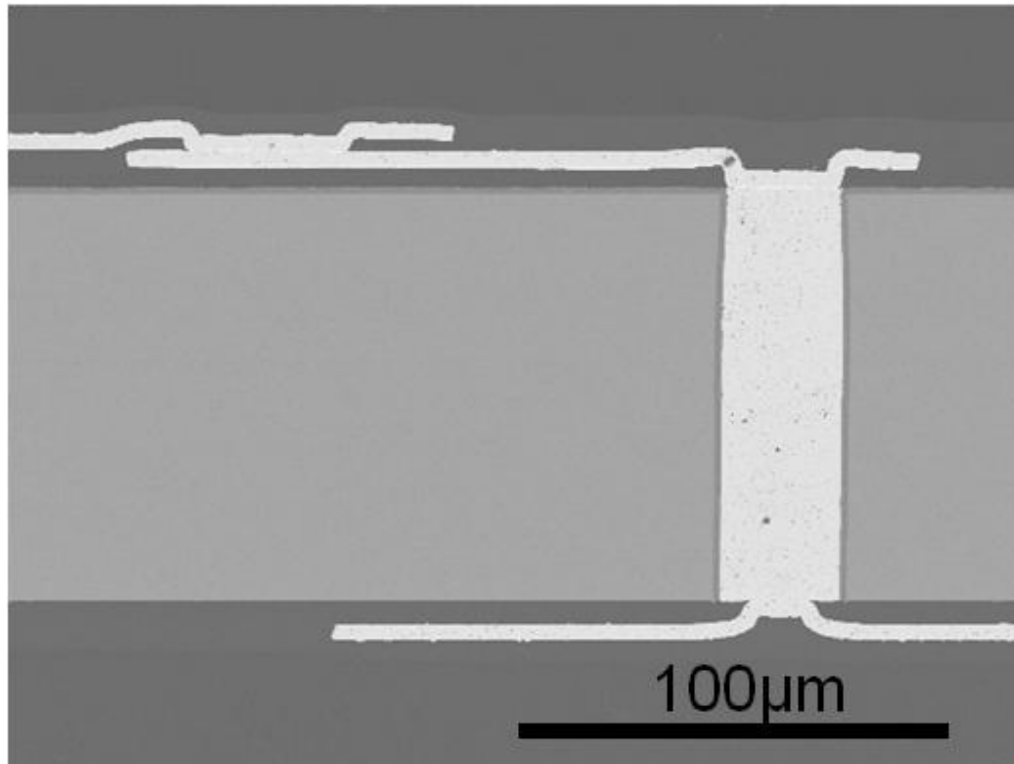
Custom Entrepix process was used to planarize Si-Ox-Cu

Polishing endpoint was determined by monitoring the exposed TSV diameter and the width of via dielectric band by microscope



Result

Completed interposer test structure: 25um via diameter, 100um thickness.
Structure has 2 frontside metal layers (4um Cu) and 1 backside metal, forming TSV chains.
Oxide / nitride TSV dielectric, polyimide dielectric on front / back wafer surfaces.



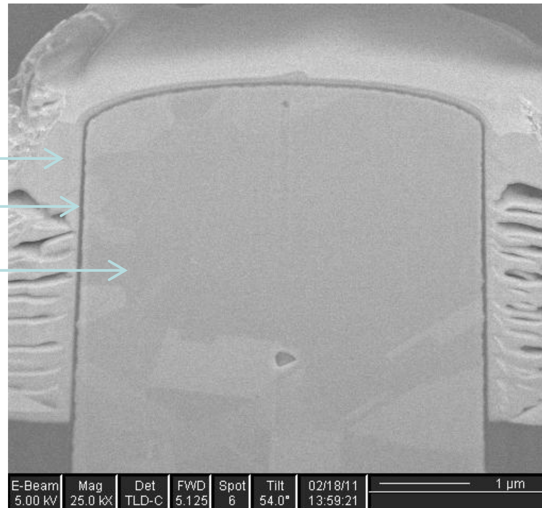
Bottom surface received TSV reveal polish

Reveal CMP #2

- After backgrind, bulk Si removed by an etch process
  - Installed equipment already available
  - Lower cost per wafer
  - Can be either dry etch or wet etch, but must be highly selective to oxide
- Si etch proceeds until 3-5um of encased via “bumps” are exposed
- Primary goal of CMP is to planarize bumps and expose the Cu cores
- One benefit of this approach is to reduce total CMP polish time (drops to roughly 1-1.5 min per platen on P1/P2 of a Mirra)
  - Less sensitive to uniformity issues
  - Faster throughput and lower cost
  - Only first pass optimization thus far … may drop even further as work proceeds

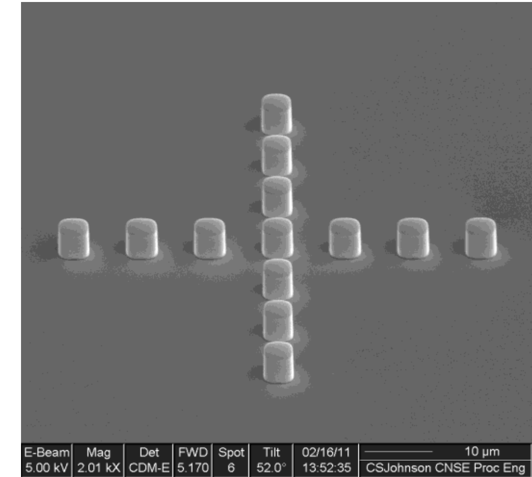
Typical After Si Etch

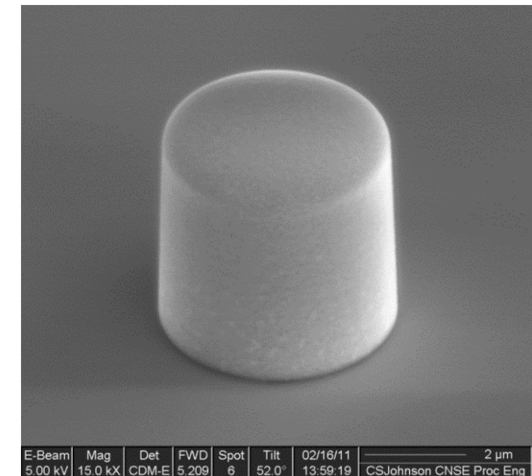
FIB Pt
Dielectric liner
Cu



FIB/SEM image of revealed via

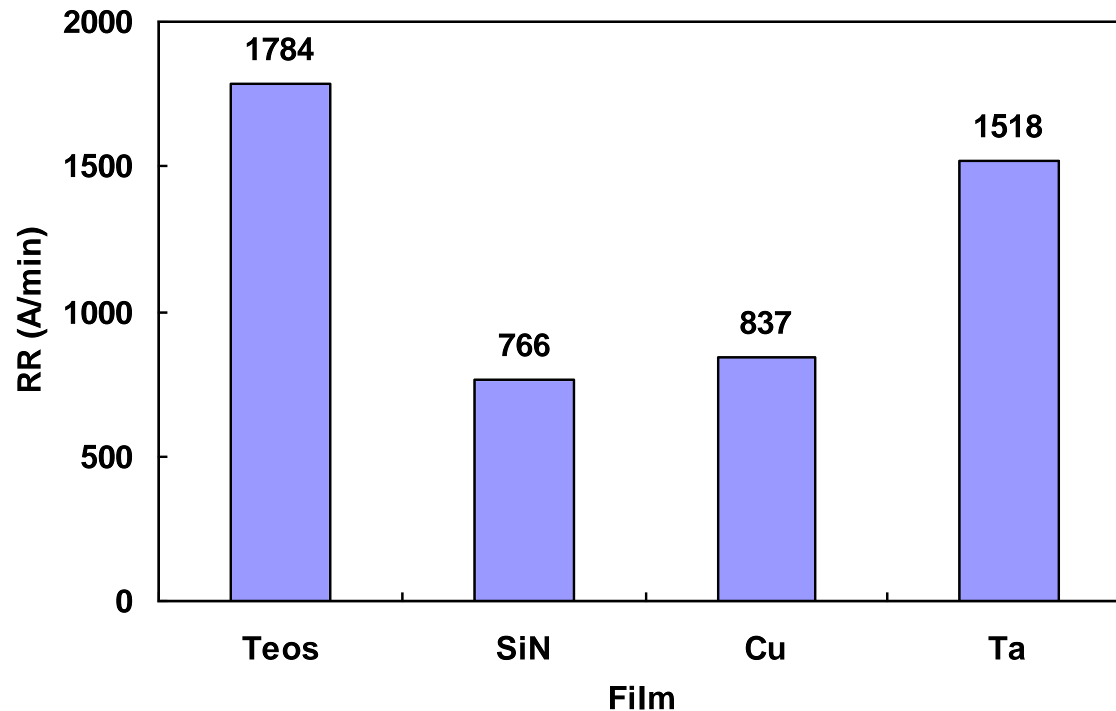
- FIB images show the dielectric liner remains intact
- No footing is observed at the base of the via
- Revealed TSVs and the Si surface are clean
- Si surface does not show pyramids or other etching defects



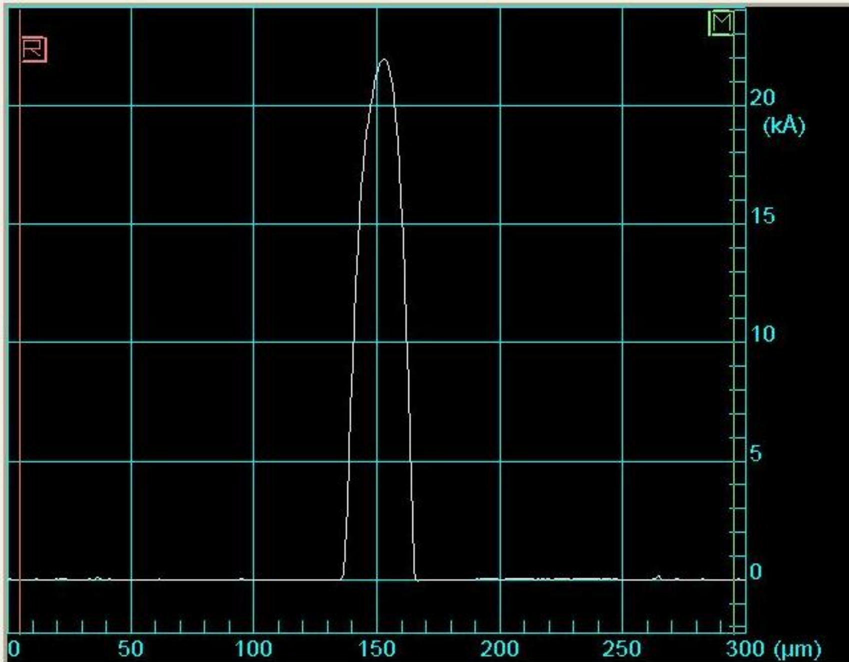


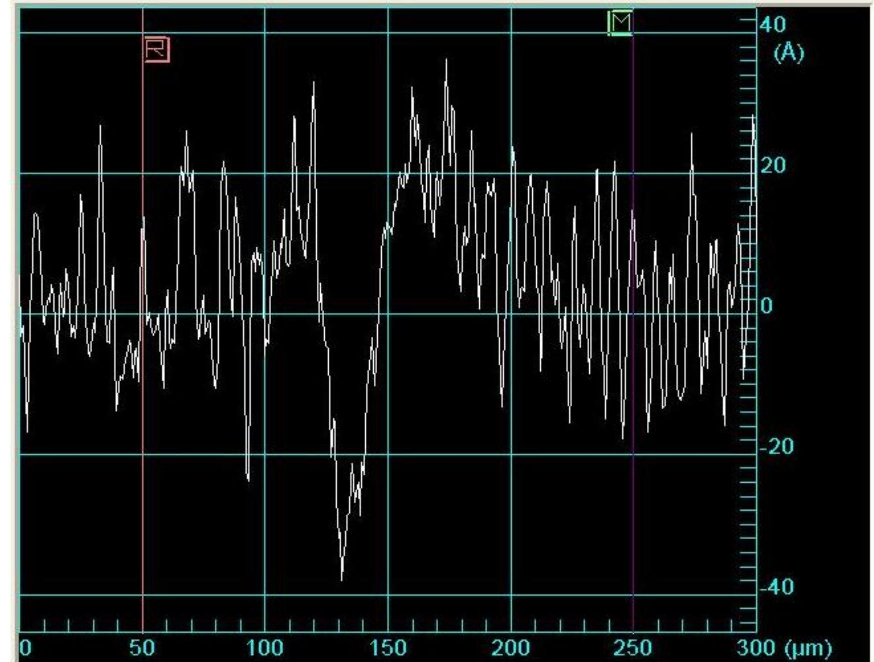
Slurry Properties

- Slurry developed by Anji (TSV-Z4) for this type of application
- Blanket film removal rates at 3psi membrane pressure
  - Effective bump removal rate is much higher due to pattern density effects



Topography – Wfr 1

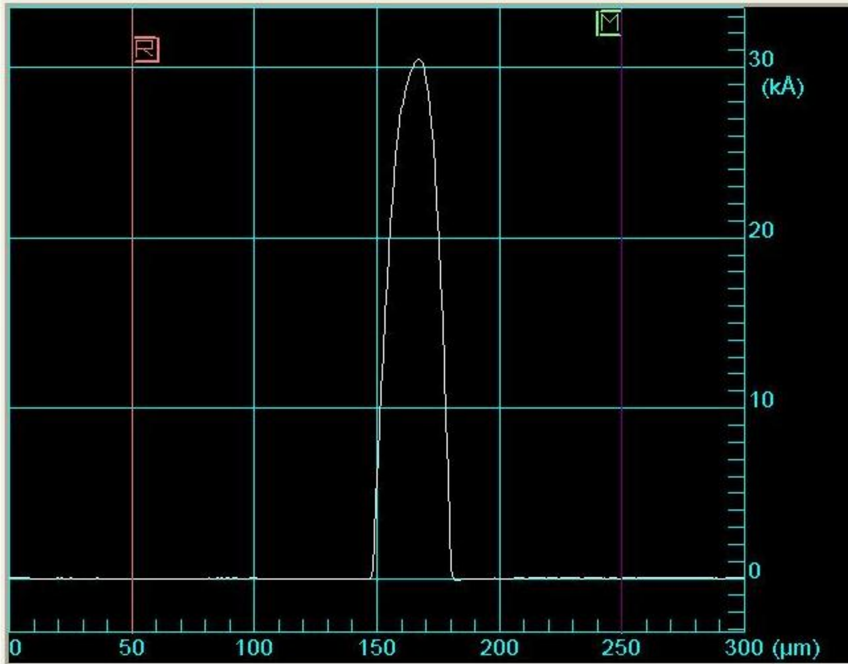


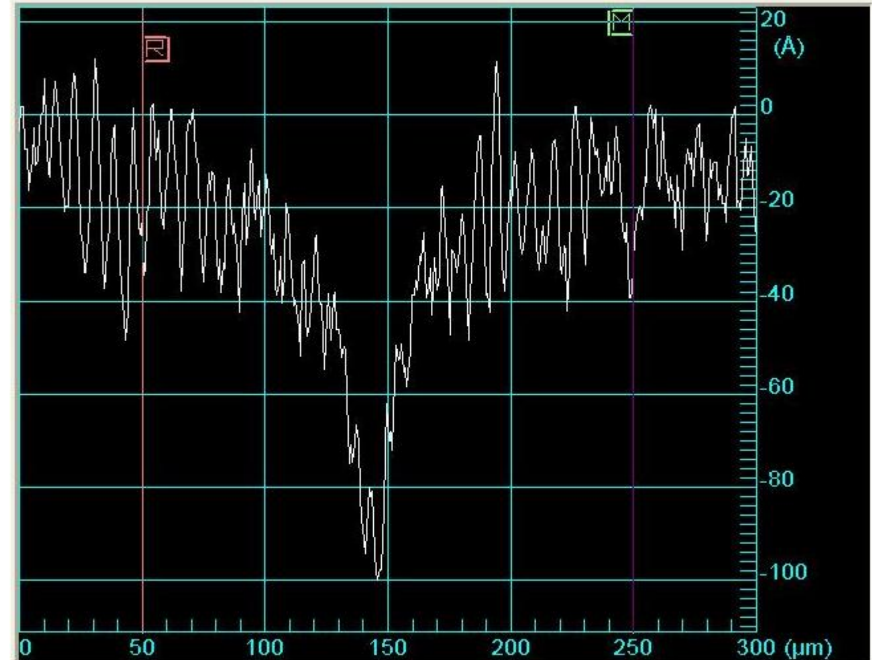


Pre-CMP Step Height
22,000 Ang

Post-CMP Step Height
60 Ang

Topography – Wfr 2





Pre-CMP Step Height
31,000 Ang

Post-CMP Step Height
100 Ang

Summary

- Single Step Non-Selective TSV Reveal
  – Custom blended formulation for high Si rate and Cu removal
  – Si removal rate >= 1 um/min
  – Low selectivity between Si and Cu (< 2:1)
  – Excellent topography control (<400 nm)
  – Single step CMP … only ONE slurry required

- TSV Reveal CMP After Highly Selective Si Etch
  – Integration demands oxide/nitride/Cu/barrier removal
  – Low selectivity among all materials
  – Excellent topography (<100 nm) and good surface finish
  – Single step CMP … only ONE slurry required

THANK YOU !

- To the following companies and individuals:
  - RTI International (Dean Malta)
  - Anji Microelectronics (Yuchun Wang)
  - Engineering Staff of Entrepix (Paul Lenkersdorfer, Donna Grannis, Terry Pfau)

- For more information, please contact:

Robert L. Rhoades, Ph.D.
Entrepix, Inc.
Chief Technology Officer
+1.602.426.8668
rrhoades@entrepix.com