Pt Vias for High Temperature MEMS Interconnects

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Abstract

A process sequence has been developed and characterized to fabricate interconnect structures in MEMS devices capable of withstanding thermal cycles up to at least 700°C. Via test structures with 3-7 μm diameter and 5-10 μm depth were etched in thermally oxidized silicon wafers and filled with platinum (Pt). Key enabling process steps are Pt electroplating and Pt CMP as reported herein. Target applications include piezoelectric MEMS or other devices requiring high temperature processing.

Introduction

Interest in 3D integration of MEMS devices continues to increase requiring integration teams to develop methods for vertical interconnects [1]. Some of these devices also require high temperature processes, such as piezoelectric layers in RF switches, cantilever sensors, and endoscopic imaging devices [2-5]. Fabricating the thru silicon vias (TSV) after these steps are completed places limitations on the overall integration. A via-first approach is strongly preferred, but requires a material capable of withstanding the high annealing temperatures required by the piezoelectric films. Platinum is a potential candidate for these applications, but fabrication techniques for Pt vias are not yet mature.

The present study reports the successful fabrication of Pt vias in a series of custom-designed test structures with a subsequent PZT piezoelectric layer deposition and anneal. The electrical and physical data from these structures indicates that a via-first TSV interconnect module based on Pt vias is plausible.

Fabrication Sequence

The objective was to demonstrate successful integration of buried platinum vias as through-silicon interconnects with a high temperature piezoelectric material, namely $Pb(Zr_{0.53},Ti_{0.47})O_3$ (PZT). Because PZT is annealed at 700°C, a non-reactive, refractory metal is required for the via metallization. Pt is a typical bottom electrode for PZT in parallel-plate capacitor configurations, so this was the primary choice for via metallization. The experimental approach was to etch vias in a silicon substrate, fill the vias with Pt metallization, and deposit PZT with bottom (Pt) and top (Au) electrodes to observe mechanical integrity of the vias and PZT after high temperature process. Furthermore, ferroelectric properties of the PZT were measured.

Silicon vias with 3 to 7 μm diameter were etched in silicon substrates using deep reactive ion etching (DRIE) to depths of 5 and 10 μm. These are fairly shallow vias with low aspect ratio (~1:1 to 3:1), but were designed to demonstrate the concept and allow ease of seed layer deposition by RF sputtering inside the vias. The wafers were then oxidized with 1 μm thermal SiO_2, and Ti seed layer was deposited with thickness of 0.5 μm by RF sputtering. In order to reduce the electrical resistivity of the seed layer, an additional seed film of 50 nm Ti and 200 nm Pt was deposited by electron beam evaporation. Negative photoresist was deposited with 3.5 μm thickness as the plating template in order to confine the plating only to the via arrays. Pt was then electroplated, followed by resist removal in solvent and chemical mechanical polishing (CMP) to provide a flat surface for subsequent PZT deposition. The bottom electrode of the PZT structure was a film stack of 25 nm Ti and 150 nm Pt deposited by evaporation. PZT was spin coated from an acetate precursor solution of Pb, Zr and Ti [6]. The film was annealed at 700°C in an O_2-rich environment and had a final thickness of 1.2 μm.

A. Pt Electroplating

One of the key steps in this effort is the deposition of sufficient thickness of Pt to fill the diameter of the via as shown in Fig 1. Electroplating is the preferred deposition

method, but a number of process parameters had to be optimized to meet the required consistency, thickness and uniformity targets. Pt plating was accomplished using a Platanex III chemistry from Enthone, Inc., which is an acidic plating chemistry designed to be used in a rack style plating system for connector and switch plating applications. Bath temperature of 75°C and pH of 1.5 are the two most important factors to monitor for this plating system in order to control the deposit and minimize the intrinsic stress of the material. An Enthone additive was used to minimize pH drift over time.

Prior to plating, the wafers were exposed to an oxygen plasma for 60 sec in order to "descum" the surfaces and improve wetting within the fine resist profile. Insufficient wetting inhibits plating in the desired features. The stress of the plated Pt film was also of utmost concern; therefore, the material was plated at a current density of 10 mA/cm^2 for a slower, more uniform deposit. For blanket Pt films, seed layer adhesion failure was observed occasionally for thicker layers due to the plated material stress, so rate control was critical. Another issue of concern was thickness uniformity across the wafer. Since the plating contact was limited to a single point along the wafer edge, the current density variation across the wafer caused a large difference in plating thickness. To overcome this effect, the plating time was split into four segments with the wafer being rotated 90° each time. This allowed for a wafer level uniformity of ±15-20% rather than the intrinsic ±40% variation. Furthermore, the additional Pt seed layer reduced surface contact resistance from 20-25 Ω for sputtered Ti only to less than 5 Ω with the Pt cap, plus an added benefit of improved plating initiation and uniformity.

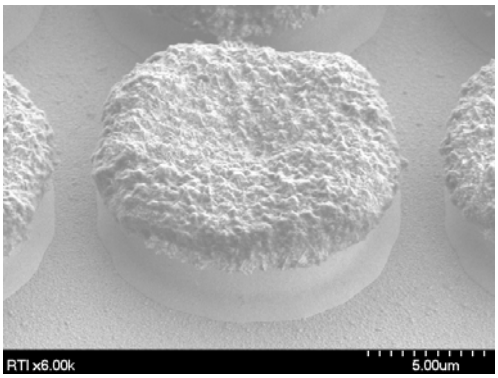

Figure 1: SEM micrograph of Pt via prior to CMP showing Pt plating overburden protruding above Si surface.

B. Pt CMP

The second key step in the fabrication of Pt vias is CMP. The requirements are high removal rate of Pt, low selectivity to Ti, high selectivity to oxide, low erosion in plug arrays, and low surface defectivity. An initial round of screening tests were performed on four slurry formulations with a series of unpatterned blanket film wafers of each material type. All wafers were polished on an IPEC 472 polisher using a pressure of 7 psi and platen speed of 60 rpm. Results are shown in Table I and Fig 2.

TABLE I
CMP REMOVAL RATE SCREENING STUDY

Slurry	Pt Rate (A/min)	Ti Rate (A/min)	Tox Rate (A/min)	Selectivity (Pt:Ti)	Selectivity (Ti:Oxide)
A	12	8	<1	1.5	> 8
B	104	1461	195	0.1	7.5
C	2980	3955	132	0.8	30.0
D	436	2108	777	0.2	2.7

As evidenced by the wide variation in removal rates and selectivities, these three materials behave quite differently with each of the four slurry formulations tested.

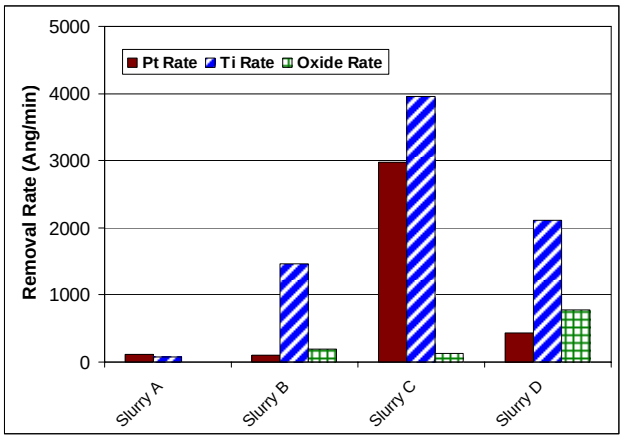

Figure 2: Graph of CMP removal rates for Pt, Ti and oxide for four different CMP slurries.

Slurry C was chosen for further process optimization then used to polish a first series of patterned wafers. As shown in Fig 3, the deposited film stack was fully cleared in 4 min 30 sec, including approximately 20% overpolish.

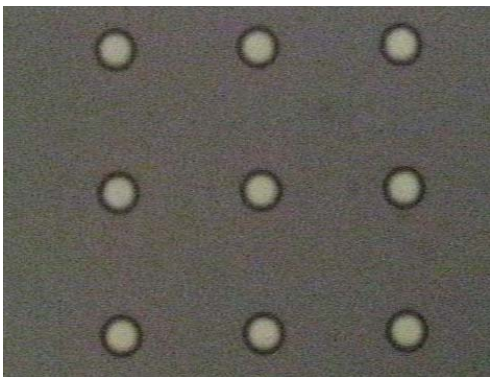

Figure 3: Microscope image (top down) of Pt vias after CMP.

Testing and Results

The Pt deposit was a completely conformal coating that successfully filled all via dimensions with void free Pt metal as seen in Fig 4 after successful CMP processing.

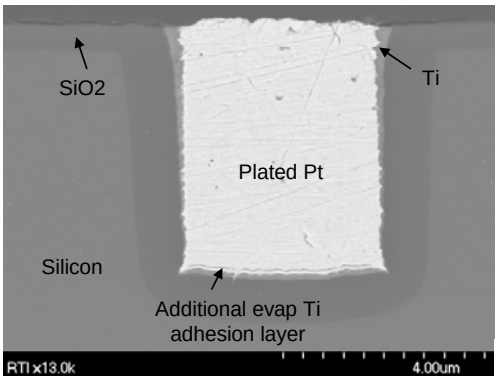

Figure 4. SEM cross section of Pt via after CMP processing.

The PZT thin film was then deposited and annealed at 700°C, yielding no cracking of the Pt plugs or the deposited film as shown in Fig 5. Minor indications of stress were observed in the deposited multilayer PZT film at the edges of the Pt plugs, but this did not cause cracking of the PZT or affect the measured electrical properties.

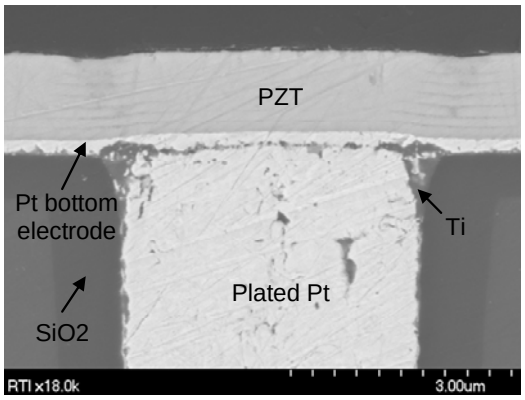

Figure 5. SEM cross section of a Pt via with PZT piezoelectric layer showing no cracking or degradation after 700°C anneal.

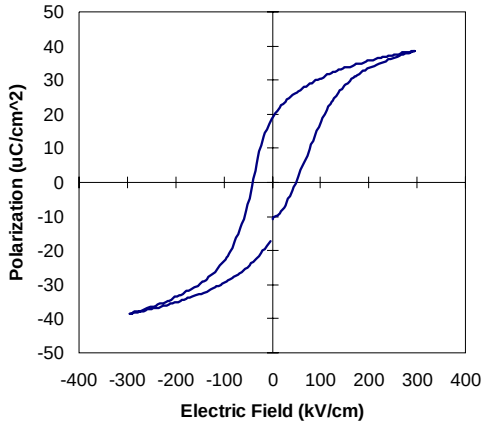

Figure 6. Ferroelectric polarization of the PZT film deposited above the plated Pt via test structures.

Ferroelectric properties were measured for the annealed PZT layer deposited over arrays of 4 to 16 Pt vias. The observed ferroelectric properties (Fig 6: remanent polarization = 18 $\mu C/cm^2$, coercive field = 44 kV/cm) in the PZT film confirmed that the PZT properties were not affected by the underlying Pt vias. Additionally, no electrical shorts were measured in the PZT film overlying the via arrays, further indicating that no defects were observed in the PZT film above the vias.

Summary

Test structures have been fabricated with Pt vias capable of withstanding a subsequent PZT piezoelectric layer deposition and 700°C anneal. Electrical and physical data from these structures confirms that a via-first TSV interconnect module based on Pt vias is plausible. Two critical process steps are required to implement this novel approach: Pt electroplating and Pt CMP. By using materials that can withstand high temperature anneals, this technology provides a path to finished MEMS devices with buried vias for subsequent 3D stacking. Further work is proceeding toward a full TSV module demonstration utilizing Pt vias to integrate finished MEMS devices with a complementary transceiver or other readout circuitry.

References

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