Planning CMP Experiments for Maximum Information at Minimum Cost

Semiconductor Equipment | Spare Parts and Service | CMP Foundry

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Introduction

General Principles

Examples

- Slurry screening
- Pad conditioning
- Repeatability / marathon
- Defectivity

Summary

Disclaimer: Comments are not intended to describe any particular person or company and are not limited to development efforts for CMOS device manufacturing. These are the personal opinions of the author and subject to change without notice. Your mileage may vary.

1. Structure the experiment to help tell a technical story
2. Have a plan and stick to it (within reason)
3. Combine types of wafers intelligently
4. Get as much data from each wafer as you can
5. Leverage previous cycles of learning (baseline data & standard cells)
6. Keep statistical rigor appropriate to the level of the work
7. Allow for fliers in the dataset, but deal with them during analysis
8. Follow the KISS rule (Keep It Simple Stupid) most of the time
9. Be observant – watch and listen (go beyond just wafer metrics)

Removal Rate and Uniformity

(includes selectivity for multiple materials)

Defectivity

Planarization

(step height, dishing/erosion, surface roughness, etc.)

Process Stability / Repeatability

(consistency from wafer-to-wafer, day-to-day, etc.)

Cost per Wafer

(key to manufacturing… and also to development)

CMP PROCESS & INTEGRATION COMPLEXITY

Wafer Parameters

- Size / Shape / Flatness
- Film Stack Composition
  - Metals (Al, Cu, W, Pt, etc.)
  - Oxide (TEOS, PSG, BPSG, etc.)
  - Other (polysilicon, low-k polymers, etc.)
- Film Quality Issues
  - Stress (compressive or tensile)
  - Inclusions and other defects
  - Doping or contaminant levels
- Final Surface Requirements
  - Ultralow surface roughness
  - Extreme planarization, esp. for CMOS
  - Low defectivity (and dropping continuously)

Pad Issues

- Conditioning optimization plays key role
- Materials (polyurethane, felt, foam, etc.)
- Properties must be chosen for the job
- Lot-to-lot consistency

Slurry Issues

- Chemistry optimization often required
- Mixing and associated inconsistency
- Shelf life and pot life
- Slurry distribution system (design, cost, upkeep)
  - Agglomeration and gel formation
  - Filtration and consistency thereof
- Cleaning method specific to slurry and materials
- Waste disposal and local regulations

Process Issues

- Long list of significant input variables
  - Downforce (and zone pressures if available)
  - Platen speed
  - Carrier speed
  - Slurry flow
  - Conditioning
    - Disk used (material, diamond size, spacing, etc)
    - Duty cycle
    - Force
    - Sweep profile
- Highly sensitive to local pattern density/pitch variation
- Must maintain consistency through pad life

Integration Issues

- Materials Compatibility
  - Electrochemical interactions with two or more metals
  - Film integrity and delamination, esp. low-k
  - Film stack compressibility
- Interactions with adjacent process modules
  - Photolithography
  - Metal deposition and metal etch
  - Dielectric deposition and etch
- Electrical design interactions
  - Feature size and spacing constraints
  - Interactions with local pattern density
  - Line resistance variation, esp. damascene copper
  - Dielectric thickness variation
  - Contact resistance variation

	CMP Process Metrics			
Process Settings	**Rate**	**Uniformity**	**Defectivity**	**Planarization**
Membrane Pressure	**STRONG**	**weak**	**Moderate**	**STRONG**
Retaining Ring Pressure	**weak**	**Moderate (strong at edge)**	**weak**	**weak**
Zone Pressures	**weak**	**STRONG**	**weak**	**weak**
Table speed, TS	**STRONG**	**Moderate**	**Moderate**	**STRONG**
Carrier speed, CS	**weak**	**Moderate**	**weak**	**weak**
Slurry flow, SF	**nonlinear**	**nonlinear**	**Moderate**	**weak**
Conditioner force	**weak**	**weak**	**weak**	**Moderate**
Conditioner speed	**very weak**	**very weak**	**weak**	**weak**

The above are only general trends … some specific processes have unusual responses
Retaining ring must be higher pressure than membrane to avoid slipout
Large delta pressure (ret ring - membrane) usually generates friction and has strong edge effect
If edge rate is low then increase the delta between CS and TS or adjust retaining ring pressure
If TS too low you won't planarize very efficiently; too high you get difficulty controlling uniformity
Typically the CS is 1 to 10 rpm different than TS - having some delta is important to avoid aliasing

CMP Development Sequence

- Generate Test Wafers
- ↓ Consumables Screening
- ↓ Process DOE's
- ↓ Optimize Uniformity
- ↓ Optimize Planarity
- ↓ Optimize Defectivity
- ↓ Repeatability (multiple runs)
- ↓ Stability (marathon)
- ↓ Release for Device Qualification

- **Sequence applies to most device integration efforts**
- **Efficiency in early stages improves with a broad range of experience with different materials, pads, disks, slurries, etc.**
- **Test wafer availability and quality often impact timeline and repeatability of results**
- **Initial process DOE's usually focus on rate and macroscopic surface quality (GRC)**
- **Optimization stages can be interchanged or executed in parallel but continue until ALL metrics are met simultaneously**
- **Effort and cost generally build through the sequence so assessments should be brutally honest**
- **And now for some examples ….**

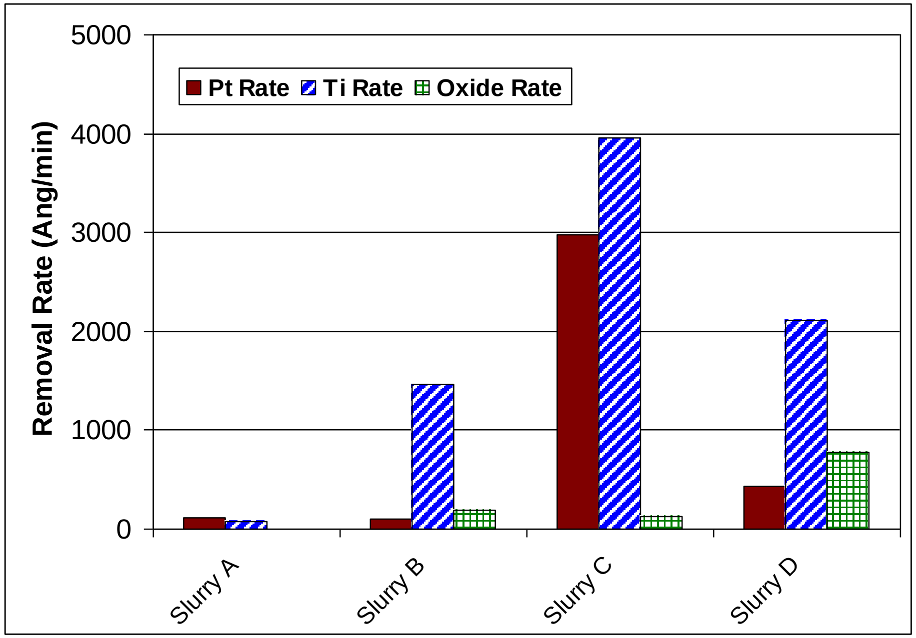
- Desired device requires high temperature processes, such as annealing of piezoelectric layers (>600°C) after via formation
- Platinum was identified as a potential candidate, but CMP for Pt vias had to be developed
- Screening expt planned with four slurries
  - Thermal oxide wafers used for pad breakin/cycling
  - Started with blanket film wafers of all exposed materials
  - Patterned wafers (limited quantity) only on best candidate

Pt Blanket Film Screening

- Screening experiments planned on blanket film wafers for removal rates and surface finish (GRC)

- Process targets:
  - Pt (RR > 2000 Ang/min)
  - Ti (RR > 2000 Ang/min)
  - SiO_2 (High selectivity)
  - Good surface quality

- Slurry C met required performance



Slurry	Pt Rate (A/min)	Ti Rate (A/min)	Tox Rate (A/min)	Selectivity (Pt:Ti)	Selectivity (Ti:Oxide)
A	12	8	<1	1.5	> 8
B	104	1461	195	0.1	7.5
C	2980	3955	132	0.8	30.0
D	436	2108	777	0.2	2.7

First run result for Pt vias

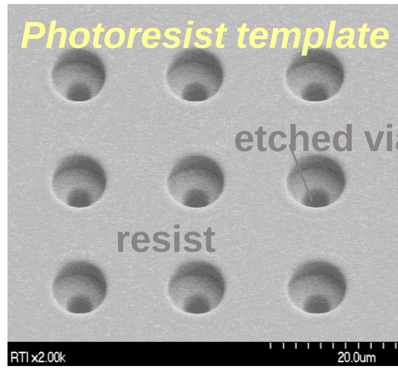
Key elements to cost savings and efficiency

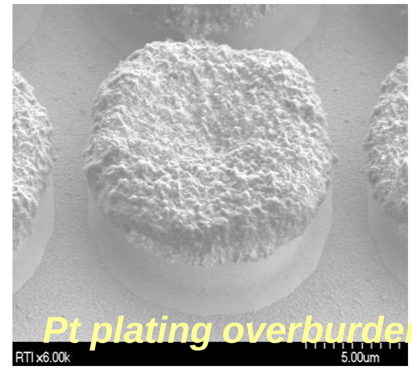
Learn as much as possible in short screening trials with a few blanket film wafers

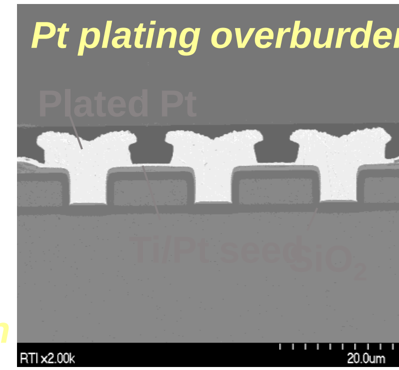
Plan 1-2 patterned wafers early to identify any “gotchas” like galvanic corrosion

Save fine tuning for later rounds

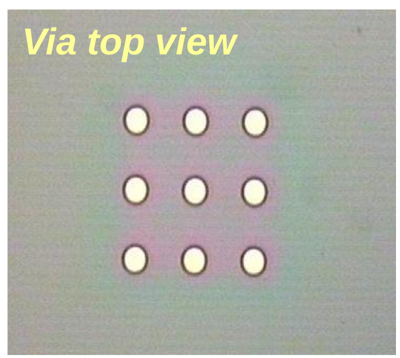
Pre-CMP

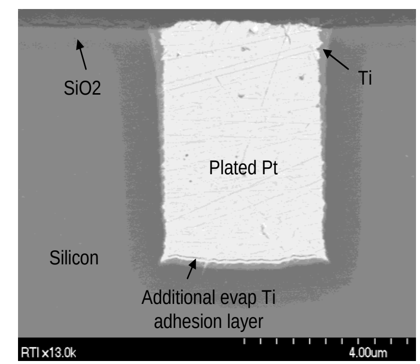


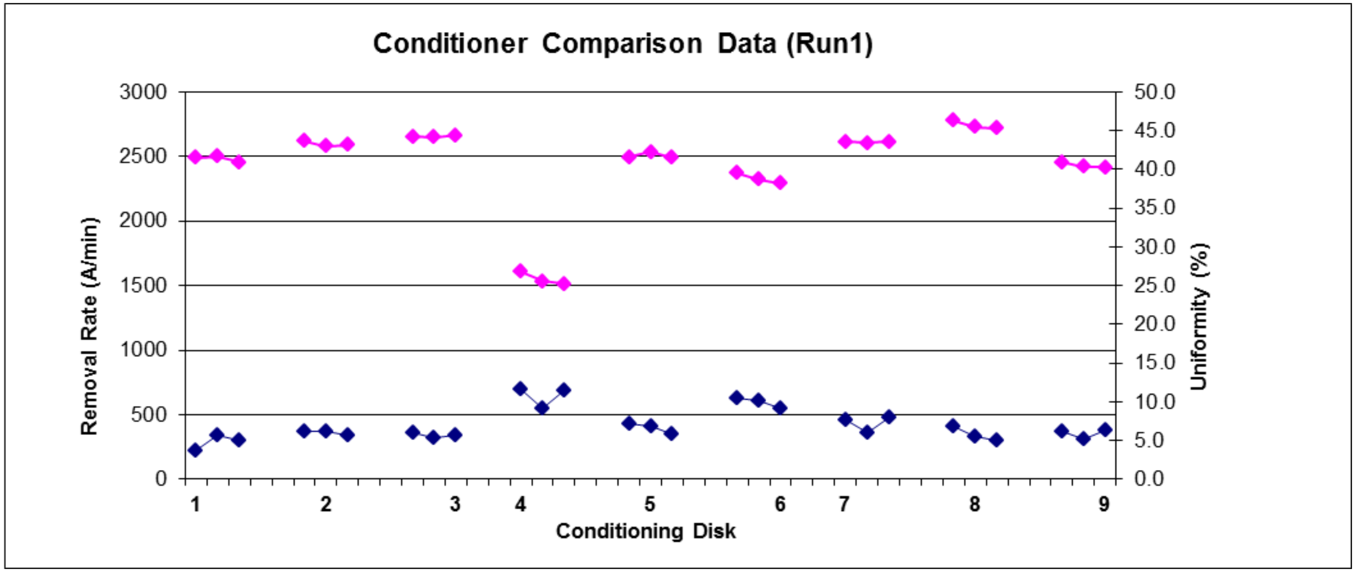


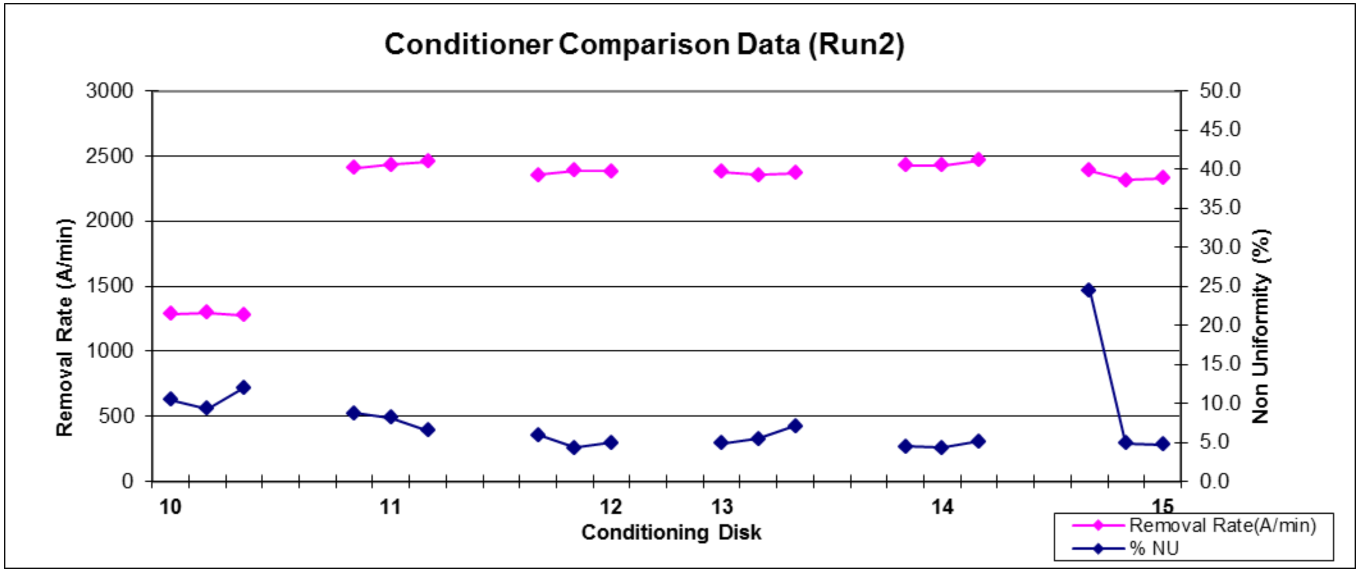


Post-CMP









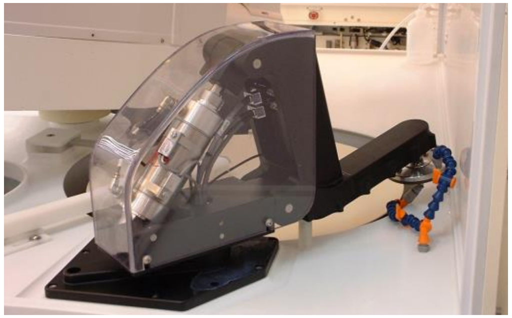
SteadySweep™ arm usng multiple brands of conditioning disks

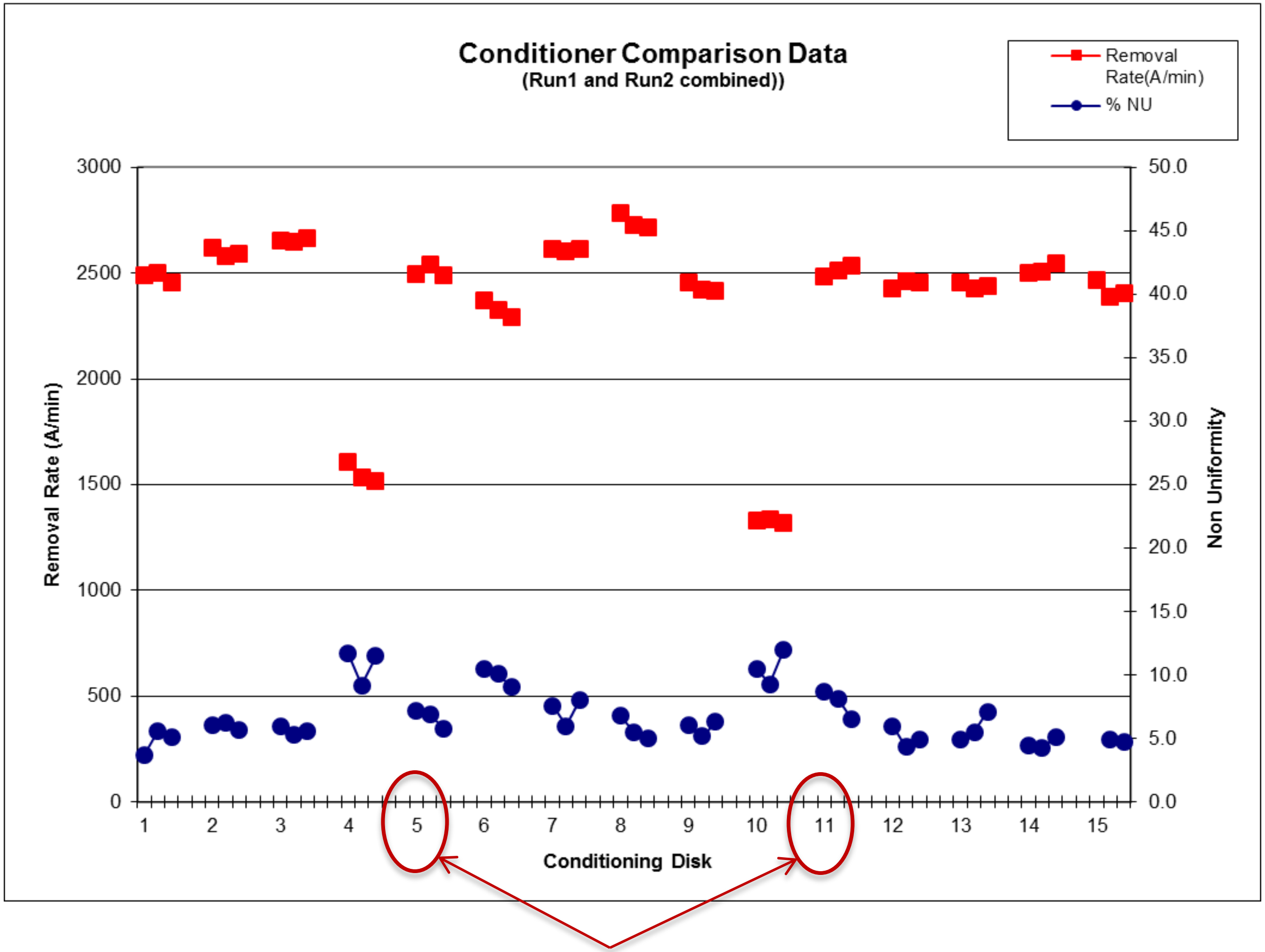
All tests within a run on the SAME IC1000

Run1 and Run2 were taken >1 year apart

<u>Expt standard cell:</u>

4 lbs cond force
15 min breakin in DIW
10 filler wafers
3 rate monitor wafers
Repeat for next disk



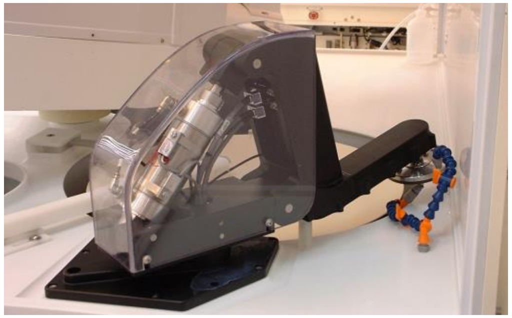


Repeat baseline disk used to stitch datasets

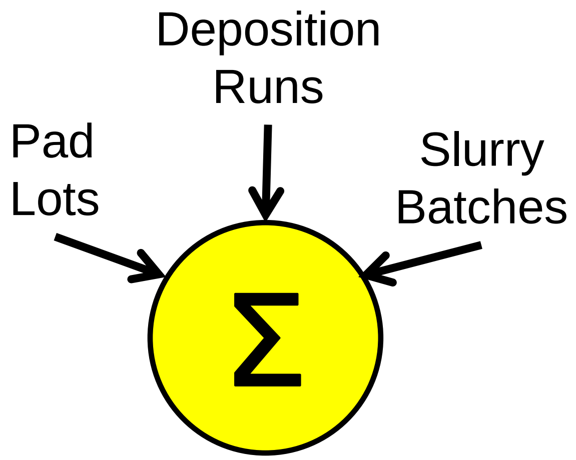
Run1Disk5 and Run2Disk2 are literally the same disk kept in a drawer in interim

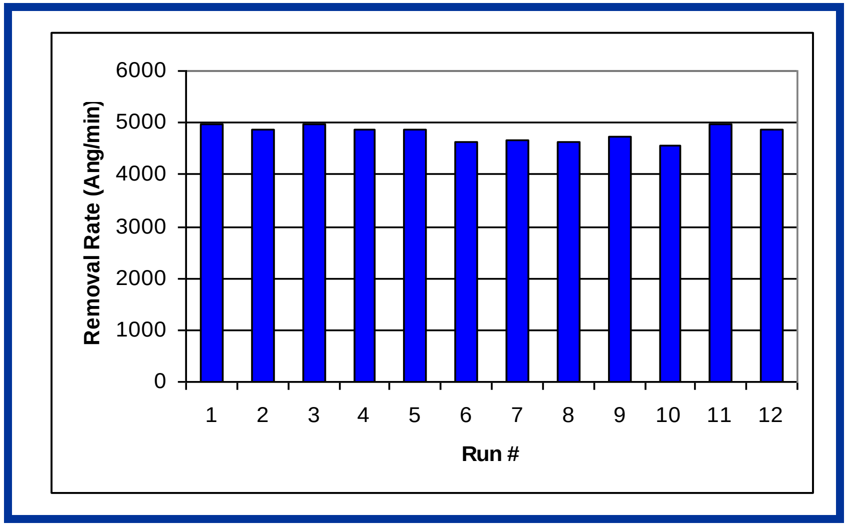
Same type of slurry and pad used, but different mfg batches

Baseline cell offset was -3.07% and used to multiply all rates in Run2 for common comparison

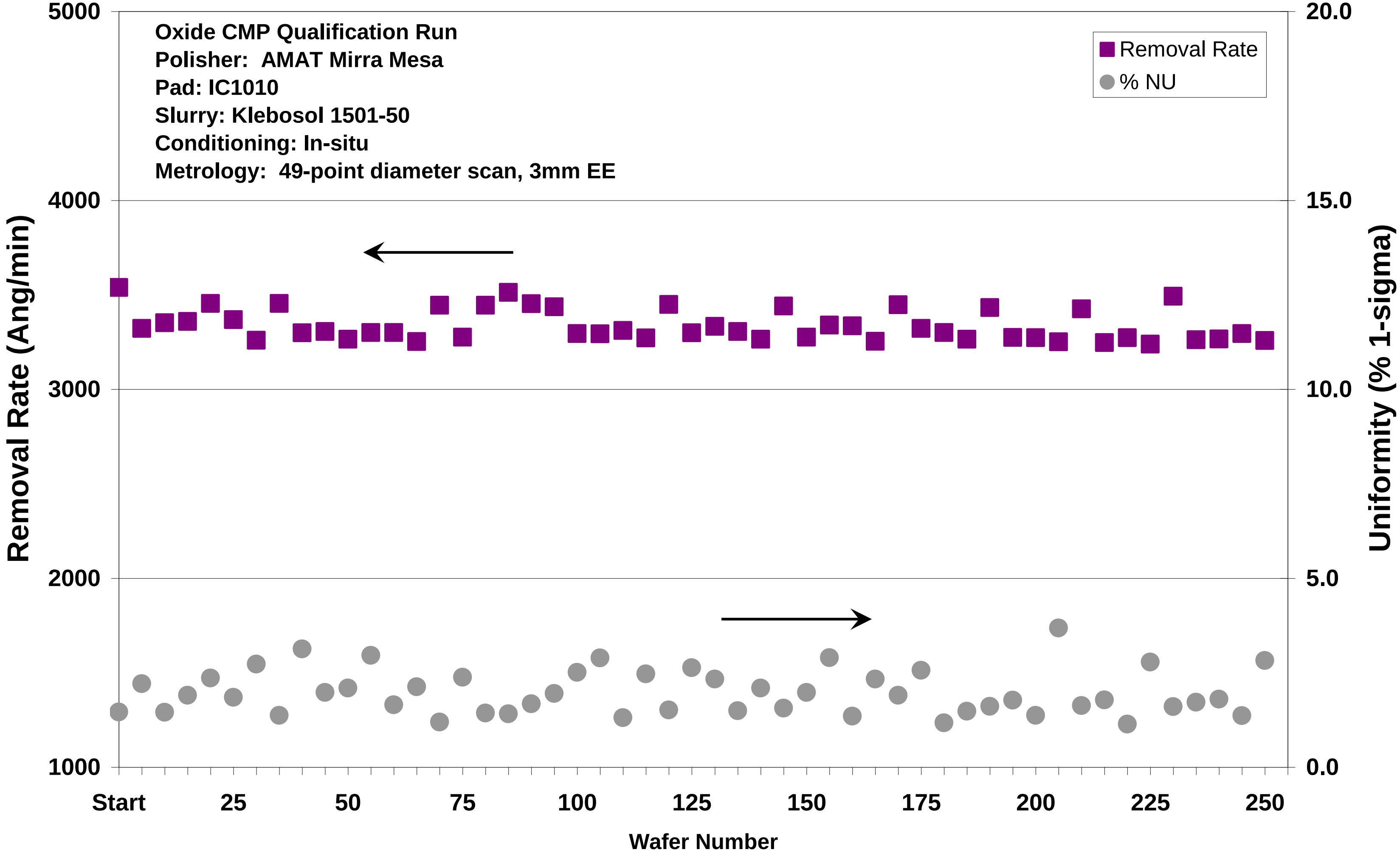


- Best approach includes multiple batches of each consumable and multiple test wafer runs
- Include "corner lots" if you want to push the process with intentional variation of inputs
- Focus on metrics that will likely be used for process quals
- Number of trials depends on degree of confidence needed
- Example at right is for multiple deposition runs of thick oxide





Oxide Marathon (Rate/Unif Every 5th Wafer)



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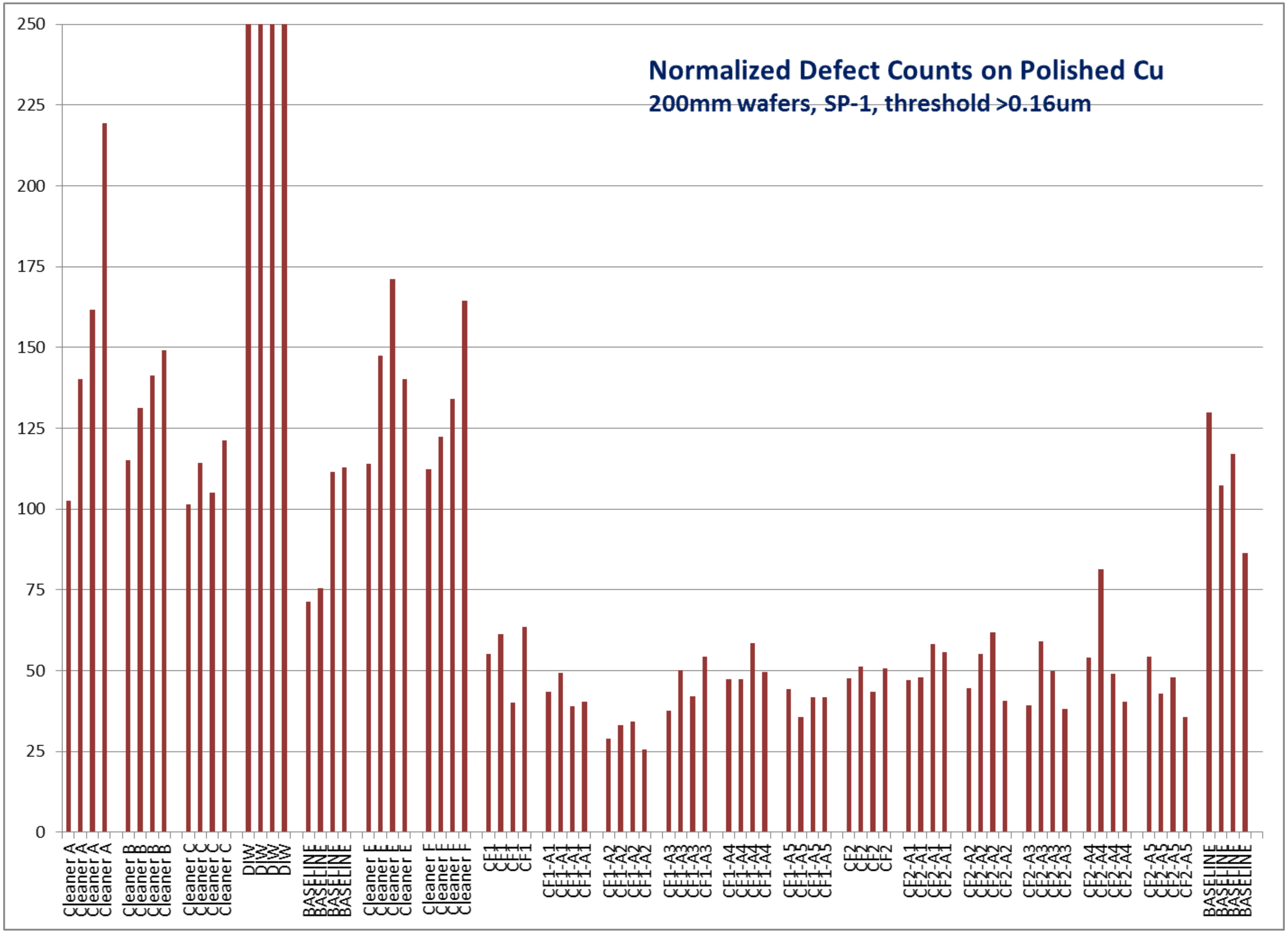
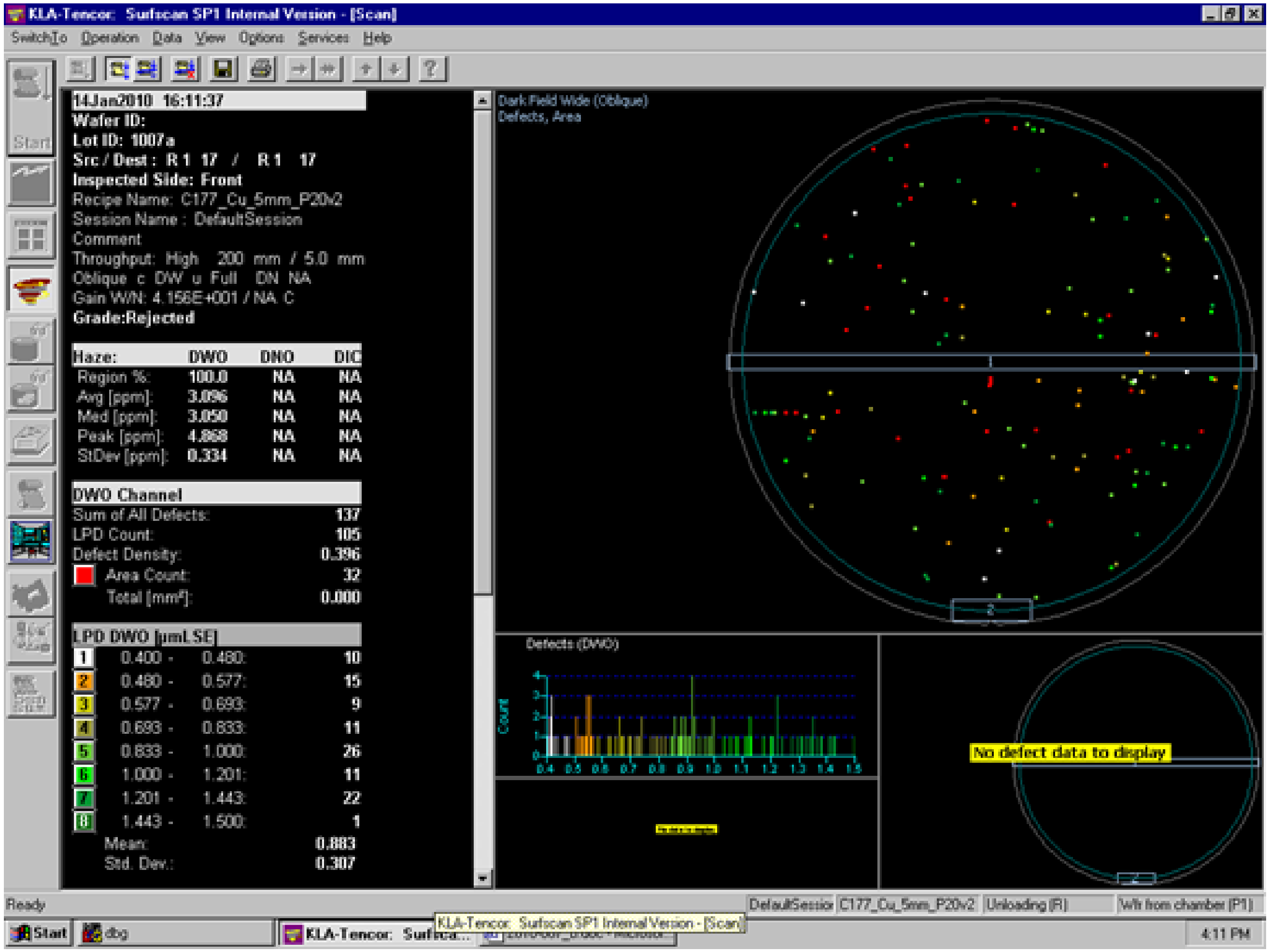
Defectivity / Baseline Cell





Traditional approach is to use a separate monitor wafer for defects … but … is this always required?

SP-1 allows custom recipe setup to ignore defined zones which only requires notch align on 4pt probe.

Example shows data for a wafer that was premeasured on 4-pt probe, then polished and cleaned, then measured for defects, and finally measured again on 4-pt probe for removal rate/uniformity

1. **Structure the experiment to help tell a technical story**
   - A mountain of data is not as useful as a few key pieces of meaningful information
   - If working on a theory or model, state that explicitly then try to prove/disprove with data
   - Use graphs and pictures to help people visualize
   - If decision at hand is a technical one, make it. If not, provide information to the decision-maker.
2. **Have a plan and stick to it (within reason)**
   - Don’t just make it up as you go – Experiments done “on the fly” are very inefficient
   - Excel spreadsheet, Gantt chart, block diagram or a napkin can all be used effectively
   - Exception to this rule: If first few wafers are clearly not giving valid data, stop and assess
3. **Combine types of wafers intelligently**
   - Thermal oxide is one of the cheapest and most consistent thin films – use it liberally
   - Once data is captured, reuse rate monitor wafers as fillers
   - Shortflows in fabs can save huge $$ by skipping unrelated process steps
   - For marathons, intersperse measured rate or defect monitor wafers between fillers
   - Lengthy trials (such as pad life studies) may benefit from quartz or other solid material wafers
4. **Get as much data from each wafer as you can**
   - Metrology is usually cheaper than more wafers and lab time
   - Save patterned wafers until end of project for possible SEM or as “show and tell” in meetings

5. **Leverage previous cycles of learning (baseline data & standard cells)**
   - Standard cells enable people running the expt to “hit a rhythm”
   - Baselines also enable efficient analysis and stitching of datasets across multiple runs
   - Can ratio all unknown conditions to the baseline cell for quick better/worse decisions
   - Repeat the baseline cell at end of a long run to catch systematic drift
   - Sometimes quickly identifies incorrect setups, hardware failures, test wafer problems, etc.
6. **Keep statistical rigor appropriate to the level of the work**
   - Early stage screening does not normally need multiple repeats – 1 or 2 wafers per cell is ok
   - Optimization requires more rigor. Suggest 3-4 wafers per cell to be able to discard fliers.
   - Repeatability trials generally need 10-30 wafers per cell to tell the difference between normal variation and something that is statistically significant
   - Remember: DOE techniques are based on an assumed LINEARITY (so don’t include slurry flow)
7. **Allow for fliers in the dataset, but deal with them during analysis**
   - It is not efficient to stop a run just to investigate one unusual data point
   - Defect counts are not a linear output variable and defect data is notoriously “noisy” which makes it difficult to analyze. Some teams use quartile analysis techniques, box-whiskers plots, etc.

8. **Follow the KISS rule (Keep It Simple Stupid) most of the time**
    - The CMP process is complex already, so keep expt design simple for cleaner data interpretation
    - For example, a series of small DOE's is preferred to one large multi-level DOE
    - Minimize the number of wafer size conversions, or pad changes, or other intrusive operations
    - Ancient wisdom: "Begin with the end in mind"
9. **Be observant – watch and listen (go beyond just wafer metrics)**
    - Color of spent slurry during polish can indicate chemical reactions or byproducts
    - Sounds can be very revealing for friction (chatter, "whale song", scraping, etc.)
    - Vibrations can be felt in frame of polisher if friction is severe, or is something is out of balance
    - Visual inspection of wafers can help identify regions for closer look in a microscope

A few comments about what NOT to do in CMP experiments

- **Avoid letting pads dry out: Dried slurry = Microscopic concrete**
- **Avoid mixing slurry chemistries or different particle types on same pad**
- **Same comment applies to PVA brushes for defectivity studies**
- **Don't polish fillers down to bare Si as it leaves byproducts on the pad** (unless the process you are working on Si or poly)
- **Don't read more into small variations than justified (esp. for defectivity)**
- **Follow the plan, but don't follow it "off a cliff" and waste the entire run**

- Thank you to the following Entrepix customers:
  - RTI International
  - ST Microelectronics
  - A few others who shall remain anonymous

- Thanks also to the Entrepix foundry team.

- For questions or additional information, please contact:

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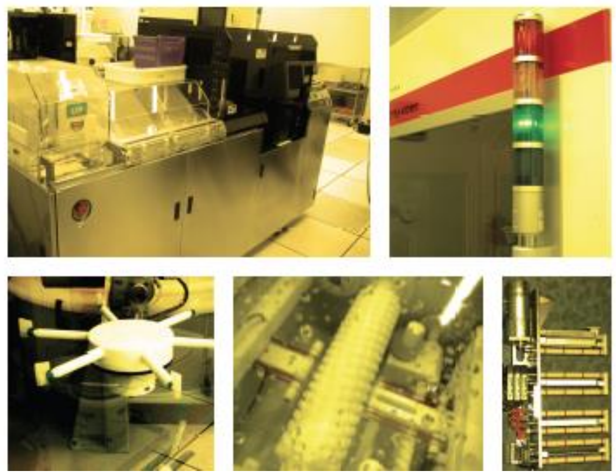

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