

CMP Historical Perspective and Future Outlook



Robert L. Rhoades, Ph.D.
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Outline



Historical Perspective of CMP

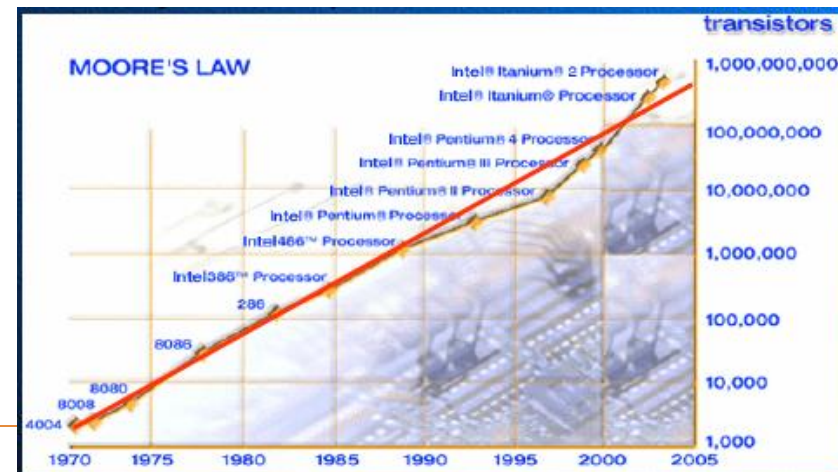
Current Trends

Future Outlook

Industry Trend



- Why are process developments so important? **SPEED and COST!**
 - New products must be ready on time for market launch
 - Long term efficiency improves competitive strength
- Moore's Law dominated the CMOS industry for >35 years
 - Not affected by cycles, markets, analysts, or the economy
- Photolithography and CMP are two critical process technologies to continue both cost and performance improvements
 - Photolithography enables SHRINKS
 - CMP enables more complex STACKS
- Trend still holds for certain industry segments, but many companies are choosing to pursue other paths



Source: Intel Corporation

Definition & Dates



- CMP = Chemical Mechanical Planarization (or Polishing)
- Adapted from optical lens polishing methods, i.e. telescope mirrors
- Timeline:
 - 1983 – Project launched at IBM Base Technology Lab in East Fishkill, NY
 - 1986 – Oxide CMP development and pilot line (IBM)
 - 1988 – Tungsten CMP development (East Fishkill and Yorktown Heights)
 - 1988 – Sematech CMP project launched and first adopters outside of IBM
 - 1992 – CMP first included in SIA roadmap
 - 1995 – Industry embraces CMP. Ramping in numerous fabs.
- CMP is now accepted as a “mainstream” process in fabs worldwide

Early Adopters & Suppliers



- Early Device Manufacturers (after IBM)
 - Intel, Micron, Motorola, Texas Instruments, National, Rockwell
- Equipment OEM's
 - Westech (later IPEC, then Speedfam-IPEC, now Novellus)
 - Strasbaugh
 - 2nd wave included Applied Materials, Ebara, Speedfam, Cybeq, etc.
- Consumable Suppliers (Initial market share leaders)
 - Slurries: Cabot, Rodel(Dow), and homebrews (IBM, Intel, etc.)
 - Pads: Rodel(Dow), Thomas West, Universal Photonics

Before & After CMP

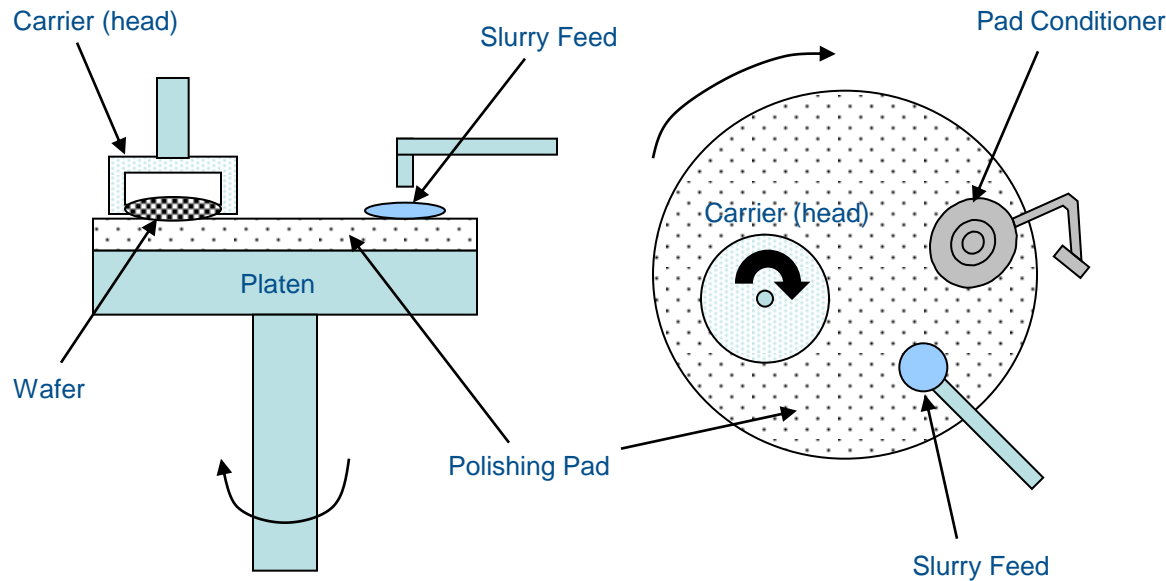


CMP = Chemical Mechanical Planarization

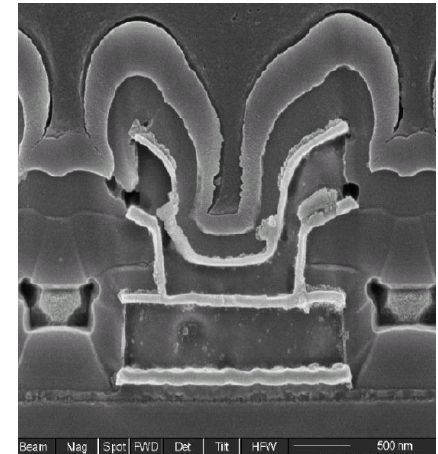
- Majority of equipment is based on rotational motion of pad and wafer (schematic representation below)
- Highest volume applications are still oxide (ILD) and tungsten CMP

(a) Side View

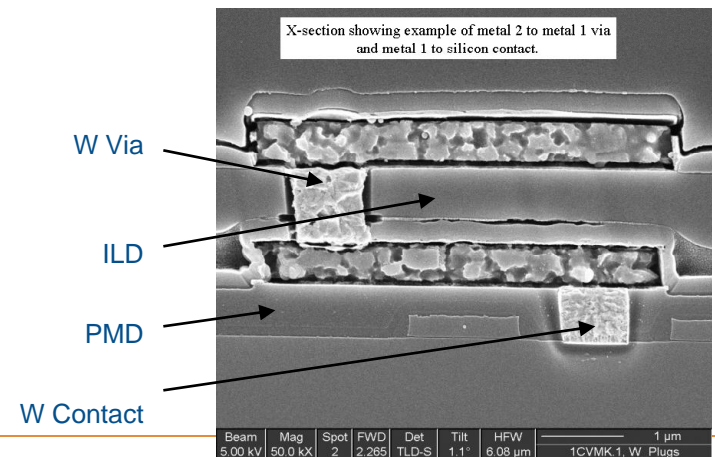
(b) Top View



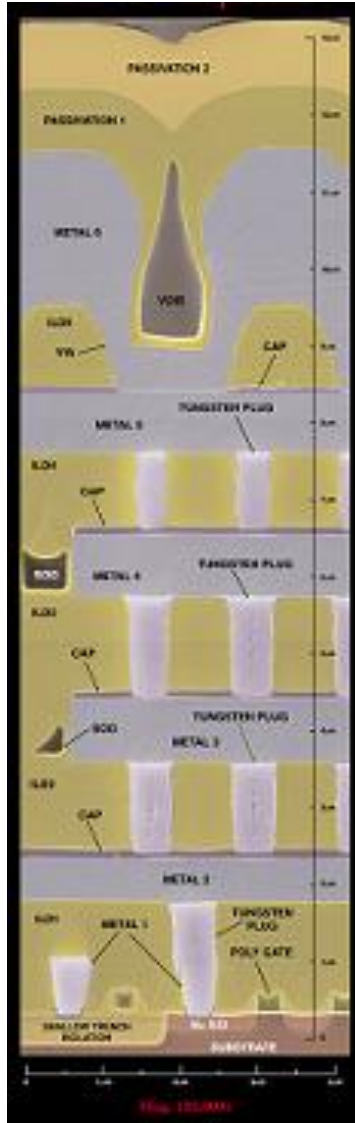
No CMP – Traditional Device



4 Basic CMP Steps – Newer Device



Life after CMP



AMD K6 microprocessor (circa 1996)

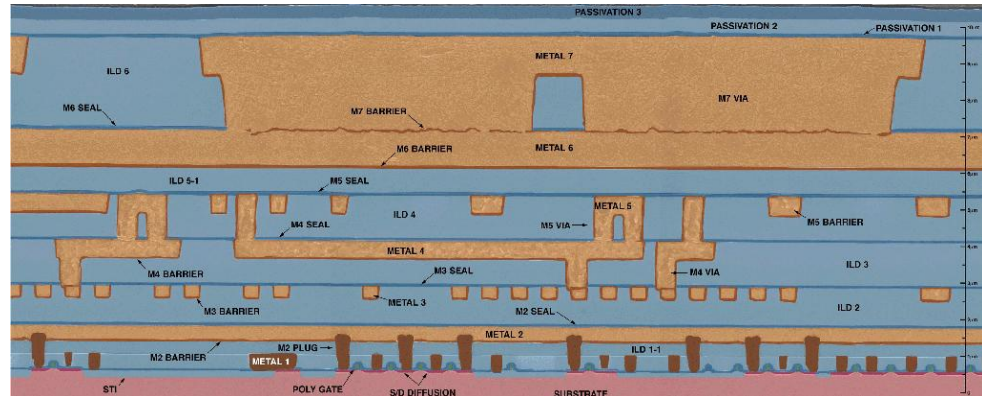
- Topography under control
- CMP enabled multiple levels of metal
- Stacked plugs no longer an issue
- Shallow trench isolation widely adopted
- Drove several generations of shrinks and more complicated stacks

- However ... this technology also started to run out of steam for the most advanced CMOS devices

And then came Cu ...



IBM PC603 microprocessor
(circa 1998)



- Dual damascene process integration for patterning Cu lines and vias
- Primary process issues: Robust clear, defect density, dishing, erosion
- Fastest growing CMP application for past few years, but still smaller than oxide and tungsten overall

Benefits of ILD CMP



- **Reduces topography for downstream processes**
 - Eliminates depth of focus issues at photo
 - Greatly reduces risk of stringers after metal etch
 - Enables stacked vias (if desired)
- **Eliminates module-to-module carryover defects**
 - CMP is sometimes called “the great eraser”
- **Provides new degrees of versatility**
 - Compatible with various etch techniques, thin metal dep, etc.
- **Stabilizes yield and improves overall process margins**
 - Especially true for interaction terms between process modules

Bottom Line: Oxide CMP addresses root cause of topography-related issues

Benefits of W CMP



- **Maintains planar surface established at ILD CMP**
- **Slurries with selectivity to oxide provide automatic polish stop**
- **Enables stacked vias**
 - Plug recess typically <20 nm (compared to 100-300nm with etchback)
 - HUGE benefit to design rules for multi-level metallization
- **Reduces module-to-module carryover defects, esp. tungsten flakes**
 - CMP is sometimes called “the great eraser”
- **Stabilizes yield and improves overall process margins**

Bottom Line: W CMP greatly improves integration of W plugs

Benefits of Cu CMP



- **Dual damascene architecture avoids need for tight-pitch Cu etch**
 - Relies on tight-pitch oxide etch instead which is much easier to achieve
- **Provides adequate control over line height consistency**
- **Provides protection of freshly polished Cu surfaces**
 - Many slurries originally used BTA to form a protective layer
 - More recent formulations use alternate means to avoid corrosion
- **Only proven metallization integration for sub-100nm design rules**

Bottom Line: Cu CMP enables sub-100nm interconnects

Mainstream CMP



The original technology drivers for CMP were (and often continue to be) related to topography issues in other process modules or with the overall process integration.

- ***Oxide CMP***

- Driver #1: Depth of focus at photo
 - Worse as linewidths shrank below 0.35 μm
 - Worse with additive topography of MLM
- Driver #2: Metal step coverage
 - Metal thinning on steep sidewalls
 - Topography induced etch effects
 - Inconsistent line resistance

- ***Tungsten CMP***

- Replaces plasma etchback
- Solves severe plug recess from overetch
- Lowers defectivity
- Improves yield
- Enables stacked vias

- ***Shallow Trench Isolation CMP***

- LOCOS isolation hit physical limits
- Shrinks below 0.35 μm required new isolation
- Original integration used reverse mask etch
 - Very sensitive alignment
 - Very expensive due to number of process steps
- Direct STI CMP required years of slurry innovation and process development, but is now proven in HVM

- ***Copper CMP***

- Driven by lack of acceptable Cu metal etch
- Early difficulties with electroplating profiles
- Cu/barrier metal forms electrochemical cell
- Introduction of low-k dielectric complicates an already difficult materials system

CMP Complexity



- **Wafer / Materials Parameters**

- Size / Shape / Flatness
- Film Stack Composition
 - Metals (Al, Cu, W, Pt, etc.)
 - Oxide (TEOS, PSG, BPSG, etc.)
 - Other (polysilicon, low-k polymers, etc.)
- Film Quality Issues
 - Stress (compressive or tensile)
 - Inclusions and other defects
 - Doping or contaminant levels
- Final Surface Requirements
 - Ultralow surface roughness
 - Extreme planarization, esp. Copper
 - Low defectivity at <0.12 um defect size

- **Pad Issues**

- Materials (polyurethane, felt, foam, etc.)
- Properties must be chosen for the job
- Conditioning method often not optimized
- Lot-to-lot consistency

- **Slurry Issues**

- Chemistry optimization often required
- Mixing and associated inconsistency
- Shelf life and pot life sometimes very short
- Slurry distribution system (design, cost, upkeep)
 - Agglomeration and gel formation
 - Filtration is often required
- Cleaning method specific to slurry and film
- Waste disposal and local regulations

- **Process Issues**

- Long list of significant input variables
 - Downforce
 - Platen speed
 - Carrier speed
 - Slurry flow
 - Conditioning method
 - Disk used (material, diamond size, spacing, etc)
 - Force
 - Speed
 - Sweep profile
- Highly sensitive to local pattern variation
- Must maintain consistency at high throughput
- Must optimize for variation of incoming films

- **Integration Issues**

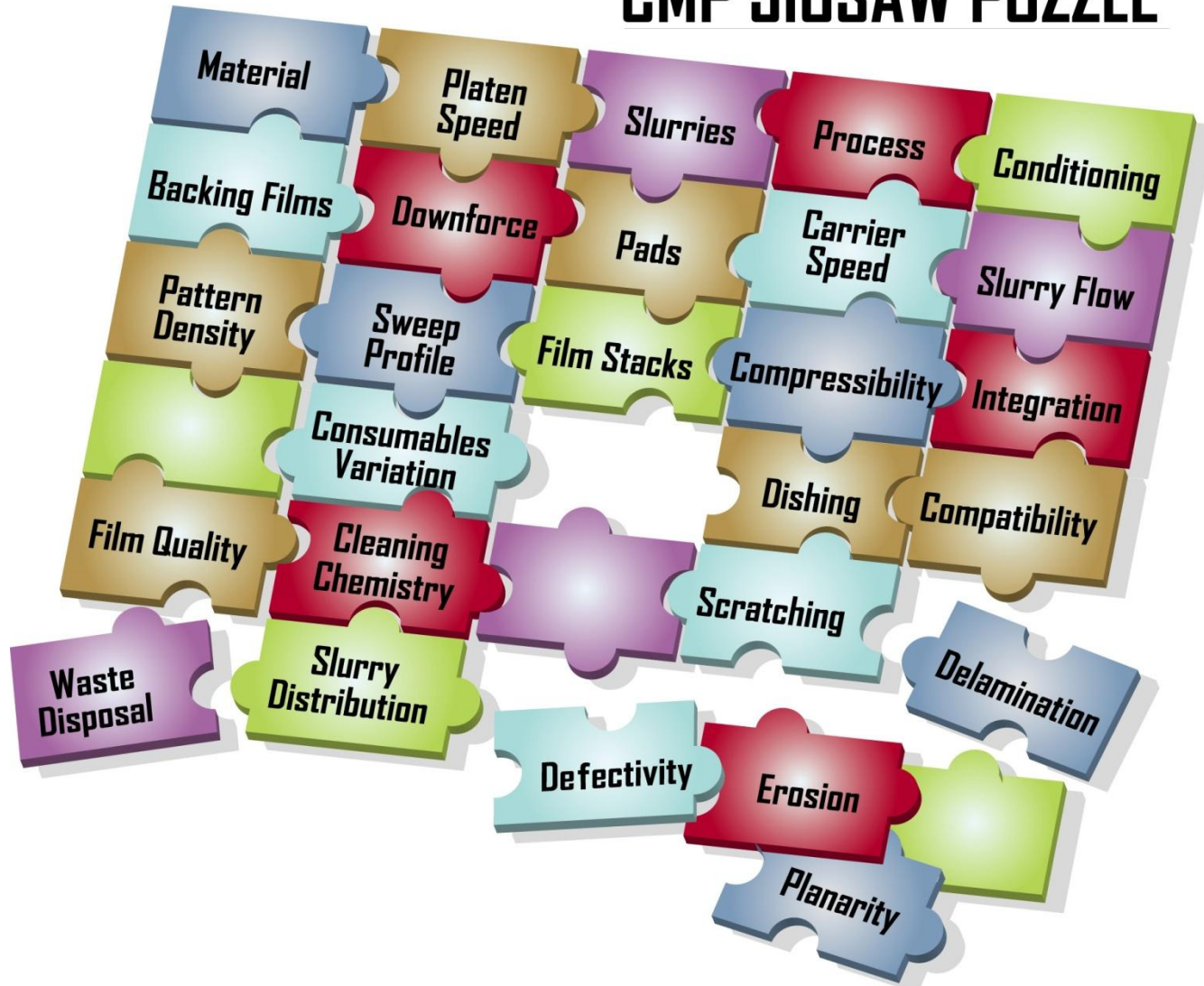
- Materials Compatibility
 - Electrochemical interactions with two or more metals
 - Film integrity and delamination, esp. low-k
 - Film stack compressibility
- Interactions with adjacent process modules
 - Photolithography
 - Metal deposition and metal etch
 - Dielectric deposition and etch
- Electrical design interactions
 - Feature size constraints
 - Interactions with local pattern density
 - Line resistance variation, esp. damascene copper
 - Dielectric thickness variation
 - Contact resistance variation

Process development teams must balance complexity, cost, risk, and timelines.

CMP Jigsaw Puzzle



CMP JIGSAW PUZZLE



Each new material or new integration usually requires a new CMP process or at least a re-optimization of the module.



Most CMP processes are measured on 5 basic metrics

Removal Rate and Uniformity

Defectivity

Planarization

(step height, dishing/erosion, surface roughness, etc.)

Process Stability

(repeatability from wfr-to-wfr, run-to-run, etc.)

Cost per Wafer

Interactions



	CMP Process Metrics			
Process Settings	Rate	Uniformity	Defectivity	Planarization
Down force, DF	STRONG	weak	Moderate	STRONG
Back pressure, BP	weak	Moderate	weak	weak
Table speed, TS	STRONG	Moderate	Moderate	STRONG
Carrier speed, CS	weak	Moderate	weak	weak
Slurry flow, SF	nonlinear	nonlinear	Moderate	weak
Conditioner force	weak	weak	weak	Moderate
Conditioner speed	don't care	don't care	weak	weak

Upscaled CMP



Upscaled CMP

Microelectronics and CMP if 1 micron were enlarged to 1 inch

Item	Actual Size	Upscaled Size	Approximate equivalent
Slurry particle	0.1 um	0.1 inch	BB or large grain of sand
Pad asperity	10-40 um	10-40 inches	Basketball to laundry basket
Pad pores (IC1000)	50-100 um	50-100 inches	Small hot tub
Diamond on a conditioning disk	80-150 micron	7-12 feet	Compact car
Oxide planarization length (typical)	4 mm	333 feet	Length of a soccer field
Device - minimum feature size	65 nm	0.065 inch	Diameter of a toothpick
Device - metal line thickness	600 nm	0.6 inch	Diameter of a grape
Device - bond pad	100 micron	8.33 feet	Tool shed footprint
Width of one average die	12 mm	1000 feet	3.3 soccer fields end-to-end
200 mm Wafer	200 mm	3.16 miles	Area covered by average airport
300 mm Wafer	300 mm	4.73 miles	Area covered by large airport
Polishing pad diameter	20-30 inches	8 miles	Area covered by a small city

Outline



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Business Realities



- Time IS Money
 - Labor cost + cycles of learning + opportunity cost
- Competition in most markets is fierce
- Quality & reliability can not be compromised
- Each process module must be efficient

Trends



- CMOS industry progression for >20 years
0.5 um → 0.35 → 0.25 → 0.18 → 0.15 → 90 nm → 65 nm → etc.
- Devices, equipment platforms, even entire fabs were identified by their “target node”
- Industry language referenced the expectations
Leading edge – mainstream – trailing edge
Early adopters – fast followers – late stage
Etc.

Changes now well underway may provide alternative ways of looking at the industry.

Industry Groupings



- Group I – The most advanced, leading edge devices
 - Wafer sizes: 300mm & possibly 450mm (future)
 - Technology nodes: 65nm, 45nm, 32nm and below
 - Materials: high k, metal gates, ULK, Cu, etc.
- Group II – Improvements to mainstream ICs
 - Wafer sizes: 200mm & 150mm
 - Technology nodes: 90nm to 350nm and above
 - Materials: oxides, tungsten, etc.
- Group III – Emerging technologies & new applications
 - Wafer sizes: 200mm, 150mm, 100mm and smaller
 - Technology nodes: various
 - Materials: wide range of metals, oxides, polymers, and more
 - MEMS, nanotechnology, SiC, GaN, optics, etc.

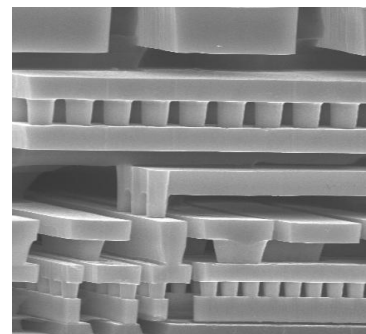
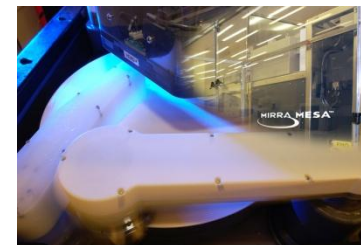


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Moore's Law

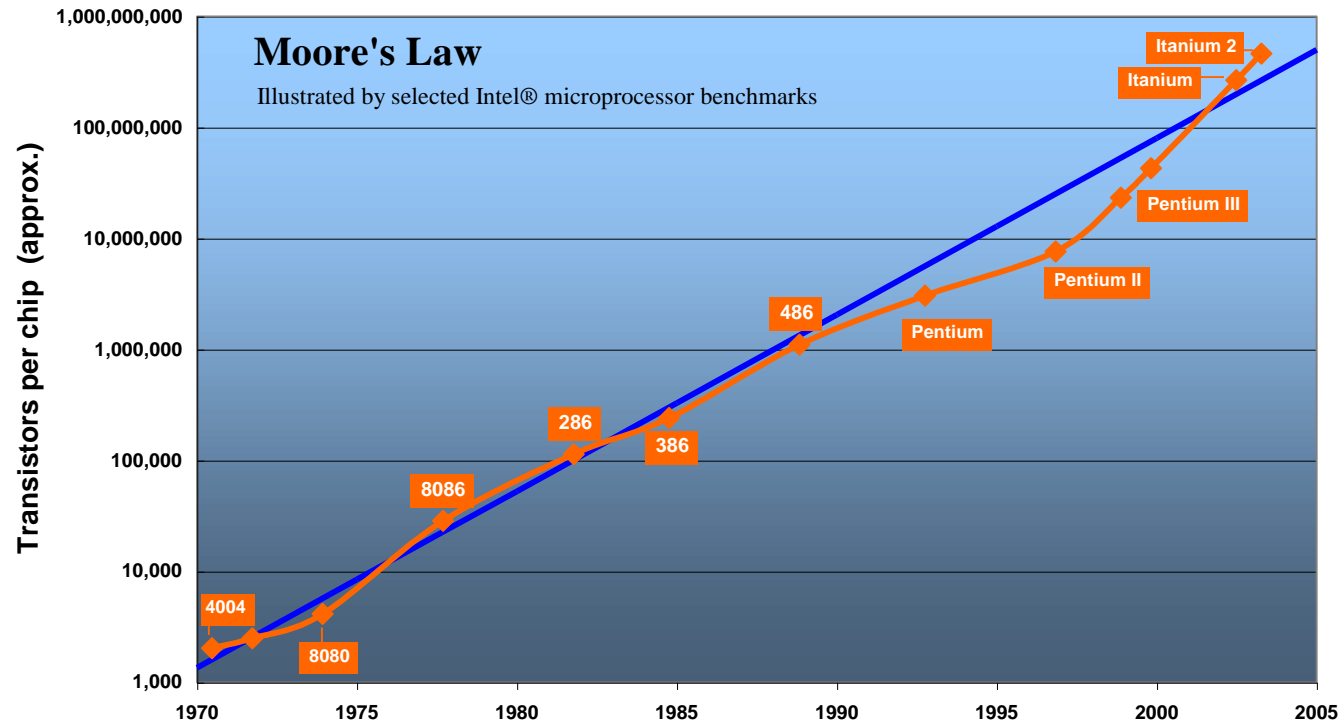


Microprocessor transistors per chip increased by over 5 orders of magnitude in 35 years.

Current generation chips have more than 2 billion transistors

Photo and CMP are 2 critical processes required to maintain the progression:

- Photo → SHRINKS
- CMP → STACKS



Moore's Law was not derailed by industry cycles, technology hurdles, or the economy ... but it does not really apply to every semiconductor company any longer ... only Group I, the "Speedsters"!

Snapshot #1



Financial Factors and Trends Across 3 Industry Segments

Financial Factor	"More Moore"		"More Than Moore"		Emerging	
	Level	Direction	Level	Direction	Level	Direction
Average Annual Capital	High	↑				
Technology R&D	High	↑				
Manufacturing Cost/chip	High	↓				
Volume	High	-				
Average Selling Price (ASP)	High	↓				

More Moore Summary



- Typical companies: microprocessor and memory makers, large-scale foundries
- Willing to spend on new fab construction (mostly 300 mm and possibly 450mm)
- Willing to adapt new materials or processes as needed to achieve performance
- Designs AND process technology both change at a rapid pace
- Design focus = performance
- Process focus = speed and acceptable yield

Snapshot #2



Financial Factors and Trends Across 3 Industry Segments

Financial Factor	"More Moore"		"More Than Moore"		Emerging	
	Level	Direction	Level	Direction	Level	Direction
Average Annual Capital	High	↑	Moderate	↓		
Technology R&D	High	↑	Moderate	↓		
Manufacturing Cost/chip	High	↓	Moderate	↓↓		
Volume	High	-	High	↑		
Average Selling Price (ASP)	High	↓	Low	-		

More Than Moore



- Wide range of products including digital, analog, mixed signal, power, etc.
- Adapting to a world of flat or falling ASP's
- Cost factors and yield are generally MUCH more important than technology factors
- Some devices enjoy long lifecycles (but not all)
- Designs may change rapidly, but process technology intentionally being held much more stable
- Design focus = features and simplicity
- Process focus = cost and maximizing yield

Snapshot #3



Financial Factors and Trends Across 3 Industry Groupings

Financial Factor	"More Moore"		"More Than Moore"		Emerging	
	Level	Direction	Level	Direction	Level	Direction
Average Annual Capital	High	↑	Moderate	↓	Low	-
Technology R&D	High	↑	Moderate	↓	High	↓
Manufacturing Cost/chip	High	↓	Moderate	↓↓	High	↓
Volume	High	-	High	↑	Low	↑↑
Average Selling Price (ASP)	High	↓	Low	-	High	↓

New Applications



CMP is still evolving for CMOS... But new applications are also being developed well beyond “traditional” CMP.

- ***MEMS***

- Oxides (doped or undoped)
- Polysilicon (often structural)
- Nitrides and oxynitrides
- Separation layer (MEMS-first or MEMS-last)
- Metals (esp. for reflective surfaces)

- ***Advanced Substrates***

- Strained layer epi substrates
- Custom III-IV and II-IV epi layers
- SOI
- AlN, diamond, GaN, GaP, SiC, etc.
- Various surfaces for direct wafer bonding

- ***Integrated Optics***

- Grating structures
- Embedded waveguides
- Integrated optical elements

- ***Other***

- Phase change memory materials
- Photoresist and other polymers
- Refractory metals
- Magnetic materials (active or shielding)
- Advanced packaging
- 3D IC's and similar device technologies

Emerging Summary



- Many products not even based on traditional CMOS
- Often adapting silicon CMOS process techniques
- Startup or new entry mentality
- Frequently start on smaller wafer sizes and transition up as production volume increases
- Integration and/or process technology are generally not mature due to some fraction of “creative” steps
- Design focus = new devices
- Process focus = acceptable yields and/or ramp

Outline




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CMP Applications



1995 - Qty ≤ 2	2001 - Qty ≤ 5	2011 - Qty ≥ 40		
CMOS	CMOS	CMOS	New Apps	Substrate/Epi
Oxide	Oxide	Oxide	MEMS	GaAs & AlGaAs
Tungsten	Tungsten	Tungsten	Nanodevices	poly-AlN & GaN
	Cu (Ta barrier)	Cu (Ta barrier)	Direct Wafer Bond	InP & InGaP
	Shallow Trench	Shallow Trench	Noble Metals	CdTe & HgCdTe
	Polysilicon	Polysilicon	Through Si Vias	Ge & SiGe
		Low k	3D Packaging	SiC
		Capped Ultra Low k	Ultra Thin Wafers	Diamond & DLC
		Metal Gates	NiFe & NiFeCo	Si and SOI
		Gate Insulators	Al & Stainless	Lithium Niobate
		High k Dielectrics	Detector Arrays	Quartz & Glass
		Ir & Pt Electrodes	Polymers	Titanium
		Novel barrier metals	Magnetics	Sapphire
			Integrated Optics	 <small>YOUR CMP PARTNER</small>

How Must CMP Adapt?



- A few common themes run across all segments:
 - Device reliability can not be compromised.
 - Quality and consistency are very important.
 - Cost is almost always a factor, though sometimes not the most important factor.
- The rest of the answers depend on which industry segment you are focused on at the time.

Future Outlook



- Future needs of the “More Moore” segment.
 - Extremely low defect levels at insanely small sizes.
 - Topography control to better than 3nm for some levels.
 - Reduce wafer-to-wafer variation.
 - CMP and cleans for new materials to solve tough physics challenges at sub-32nm design rules.
 - Tunable consumables that allow integration teams flexibility to alter rates and selectivities.
 - No longer sufficient to design for a node – fabs are unique
 - Only a small number of companies are still in this game, but wafer volumes are high at each one.

Future Outlook



- Future needs of the “More Than Moore” segment.
 - Reduce cost per wafer polished.
 - Lower defects (but only when it improves yield).
 - Stable or incremental improvements in performance.
 - New product families are generally based on same or similar process flow in existing fabs.
 - Adapt existing equipment first, whenever possible, to avoid buying new tools.
 - Large broad base of users, but conversion to a new consumable requires justification (ROI).



- Future needs of the “Emerging” segment.
 - Materials and process challenges can be very unique.
 - Volumes tend to start low, but some devices ramp fast.
 - Not as cost sensitive during development (comes later).
 - Defect levels vary wildly depending on the product.
 - Generally more willing to try new consumables.
 - Companies include a wide range from new startups to other industries to specialized development teams within major semiconductor manufacturers.

Thank You !!



**Anyone desiring a copy of this presentation
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Rob Rhoades
Chief Technology Officer
Tel: 602 426-8668
Fax: 602 426-8678
rrhoades@entrepix.com